TDA 1085

PLESSEY
Semiconductors

TDA1085C

PHASE CONTROL INTEGRATED CIRCUIT

The TDA1085C is a silicon integrated circuit designed for use in phase control systems of AC mains with resistive and inductive loads. The circuit may form the basis of closed loop control systems utilizing tacho frequency or analogue voltage feedback.

The circuit was primarily designed for motor speed control in automatic washing machines and hence includes a programmable multiple ramp generator to control acceleration rates.

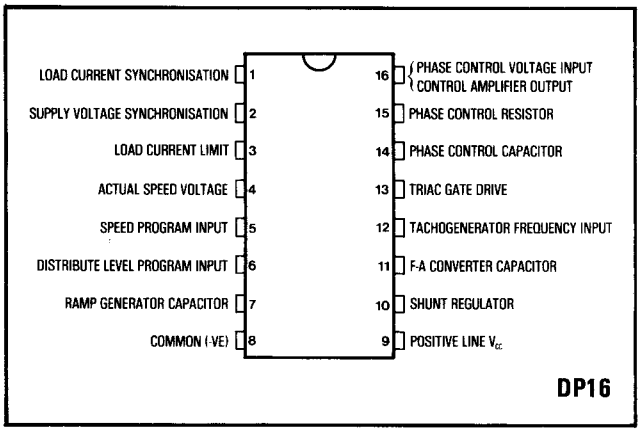


Fig.1 Pin connections - top view

SPECIAL FEATURES

- Powered direct from AC mains or DC line.
- Flexible ramp generator to provide controlled acceleration and distribution period.
- Actual speed derived from tachogenerator frequency or magnitude.
- Control amplifier allowing loop gain control.
- Symmetrical positive and negative wave firing of the triac.
- Motor current limiting.
- Fail safe in case of open circuit tachogenerator.
- Repeated triac pulses provided if triac unlatches.

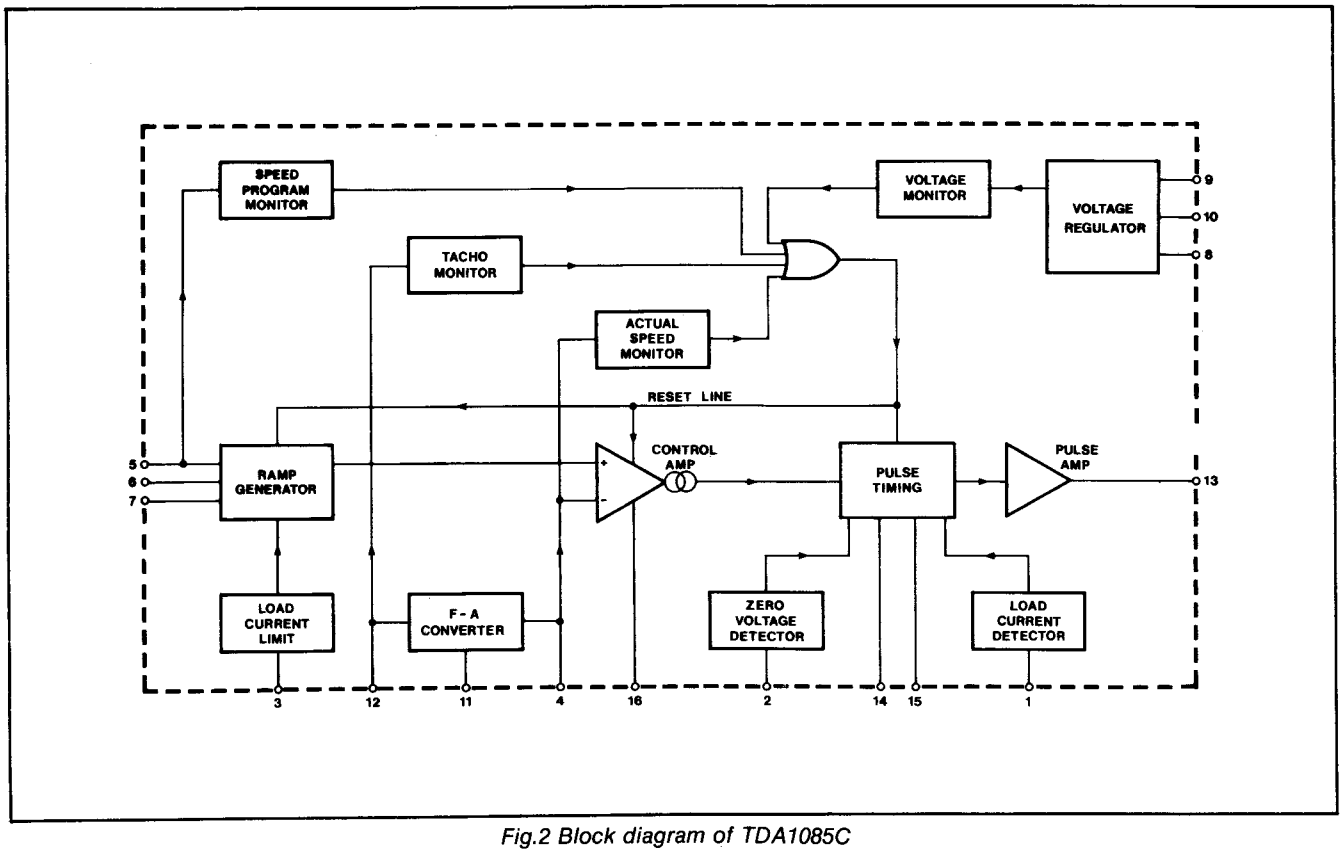


Fig.2 Block diagram of TDA1085C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$
All potentials measured with respect to common (Pin 8)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CURRENT CONSUMPTION					
Pin 9					
IC operating current		7.4	8.9	mA	Total current required is dependent on external circuitry.
VOLTAGE REGULATOR					
Pin 9					
Shunt regulating voltage		15.5	16	V	$I_9 + I_{10} = 10mA$
Monitor enable level		15.1		V	
Monitor disable level		14.5		V	
RAMP GENERATOR (See Fig.3)					
Pin 7					
Fast ramp current		1.2		mA	
Residual charging current		5		μA	During slow ramp period
Pin 5					
Speed program voltage range	0.08		13.5	V	
Bias current			-20	μA	
Pin 6					
Program distribute level	0		4	V	
Bias current			-20	μA	
Internal					
Low distribute level V_{RA}		V_6	1.2	V	Distribute levels referred to ramp generator.
High distribute level V_{RB}	$1.9V_6$	$2V_6$	$2.1V_6$	V	
FREQUENCY-ANALOGUE CONVERTER					
Pin 12					
Positive tacho input voltage			6	V	
Negative tacho input voltage			-3	V	
Minimum tacho input voltage	200			mV	Peak-Peak
Internal bias current		25		μA	
Pin 12 to Pin 11					
Conversion factor (typical)		7.5		mV/Hz	C pin 6 = 390pF,R pin 4 = 150kΩ
		15		mV/Hz	C pin 6 = 820pF,R pin 4 = 150kΩ
Conversion gain		10			
Linearity		±4		%	
CONTROL AMPLIFIER					
Pin 4					
Actual speed voltage limits	0		13.5	V	
Analogue input bias current			-350	nA	
Pin 4, 5 & 16					
Differential offset voltage	-60		+20	mV	$V_5 - V_4$ to give $I_{16} = 0$
Transconductance		300		μA/V	
Pin 16					
Output current drive		±100		μA	
FIRING PULSE TIMING					
Pin 2					
Voltage sync trip level		±50		μA	
Pin 1					
Current sync trip level		±50		μA	
Pin 16					
Phase control voltage swing		11.7		V	
Pin 13					
Firing pulse width		55		μs	R pin 15 = 300kΩ
Pulse repetition time		200		μs	C pin 14 = 47nF
Pin 14					
Ramp recharge current (I_R)		150		μA	
FIRING PULSE OUTPUT DRIVE					
Pin 13					
High output level		$V_{CC} - 4$		V	At 150mA drive current
Leakage current			30	μA	

(continued)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
LOAD CURRENT LIMITER					
Pin 3 & Pin 7					
Current gain		170	—		Reset of ramp generator
Pin 7					
Discharge current		35		mA	

CIRCUIT DESCRIPTION

The TDA1085C incorporates a shunt type voltage regulator which enables it to be powered direct from the mains or from a DC supply. It can provide adequate current to drive external speed reference potential dividers that may be switched by contacts on mechanical timers. A supply monitor circuit resets timing functions and inhibits triac firing pulses when the circuit is being powered up at 'switch on'.

A ramp generator is provided to control the acceleration of the motor, to a speed as programmed on the speed program input, pin 5. If this pin becomes grounded a general reset and inhibit of triac pulses will take effect. A programmable period of slow acceleration may be used to give a 'distribution' period for automatic washing machines. Charging currents for the ramp generator are determined by an external resistor for the slow ramp period and internally during the fast ramp.

A frequency to analogue (F-A) converter is provided on this device enabling advantage to be taken of tachogenerator frequency to be used for motor speed sensing. The conversion is carried out by transferring a pulse of charge (defined by the F-A converter capacitor) into an RC filter when the tacho input goes positive. An internal bias current is provided to the input pin; this serves two purposes: it senses the continuity of the tacho, causing a general reset and inhibit of output pulses if it goes open circuit; secondly it enables the input to be easily biased such that tacho noise causes no additional triggering of the F-A converter.

The control amplifier has differential inputs that compare the ramp generator voltage (internal) against the actual speed voltage. The output of this amplifier is a bidirectional current of limited amplitude which is integrated to limit the maximum rate of change of triac firing pulse phase angle. The actual speed voltage may be derived directly from a tacho (for analog sensing) or via the F-A converter circuit (for digital sensing). Digital sensing has the advantage that no tacho calibration is required, plus stability against temperature variations and ageing effects.

Synchronisation of the triac pulse is achieved by delaying the pulse with reference to the zero voltage points of the mains cycles. These points are determined by the voltage synchronisation input to the device. Inductive motors give rise to phase lag of the load current. Under high speed or heavy load conditions it is essential that the triac is fired after the load current from the previous half cycle has ceased. The current synchronisation pin (1) performs this task by ensuring that there is a voltage across the triac before a trigger pulse is supplied (when the triac is conducting current only a small voltage drop appears across it). The triac pulse width is dependent on the capacitor which also delays the pulse from the zero voltage point. If the triac fails to latch, repeated pulses will be supplied.

The current limitation pin (3) may be used to monitor the peak negative load current. This may be necessary to protect the triac and or motor under stall conditions. The trip point is determined by external resistors which when exceeded will cause the ramp generator to discharge to a safe working voltage.

RAMP GENERATOR CHARACTERISTIC

V_{RA} and V_{RB} are determined by the voltage programmed on pin 6 (V_6). Under all conditions $V_{RB} = 2V_6$, whereas $V_{RA} = V_6$ for $V_6 \leqslant 1.2V$ but is clamped at 1.2V for $V_6 \geqslant 1.2V$.

The ramp generator output voltage only rises to the desired speed voltage as defined on pin 5.

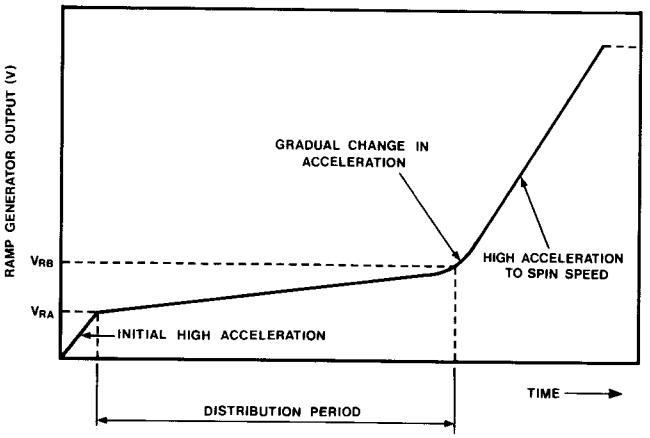


Fig.3 Ramp generator characteristic

ABSOLUTE MAXIMUM RATINGS

Electrical

Peak input current (I sync), pin 1:	±2mA
Peak input current (V sync), pin 2:	±2mA
Current drain, pin 3:	-5mA
Positive input voltage, pin 3:	6V
Analog voltage drive, pin 4:	V_{CC}
Speed reference voltage, pin 5:	V_{CC}
Distribute level, pin 6:	V_{CC}
IC Circuit current (pin 10 disconnected), pin 9:	10mA
Supply shunt regulating current, pin 10:	30mA
Tachogenerator (digital) drive input, pin 12:	-3, +0.1mA
Triac gate current, pin 13:	200mA
Phase timing current, pin 15:	1mA

Thermal

Operating ambient temperature:	0°C to +70°C
Storage temperature:	-55°C to +125°C

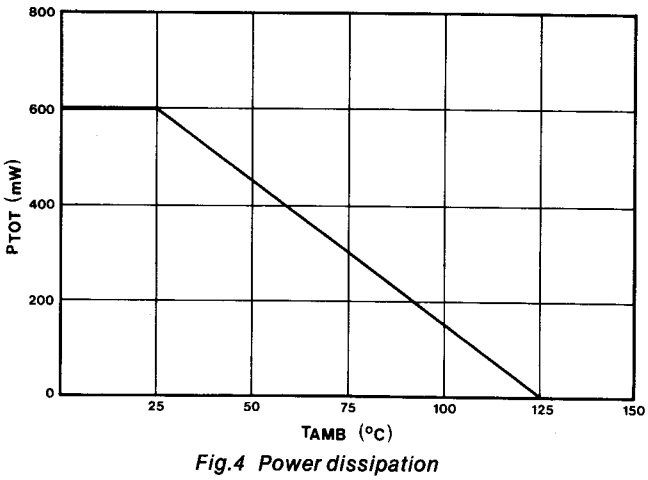


Fig.4 Power dissipation

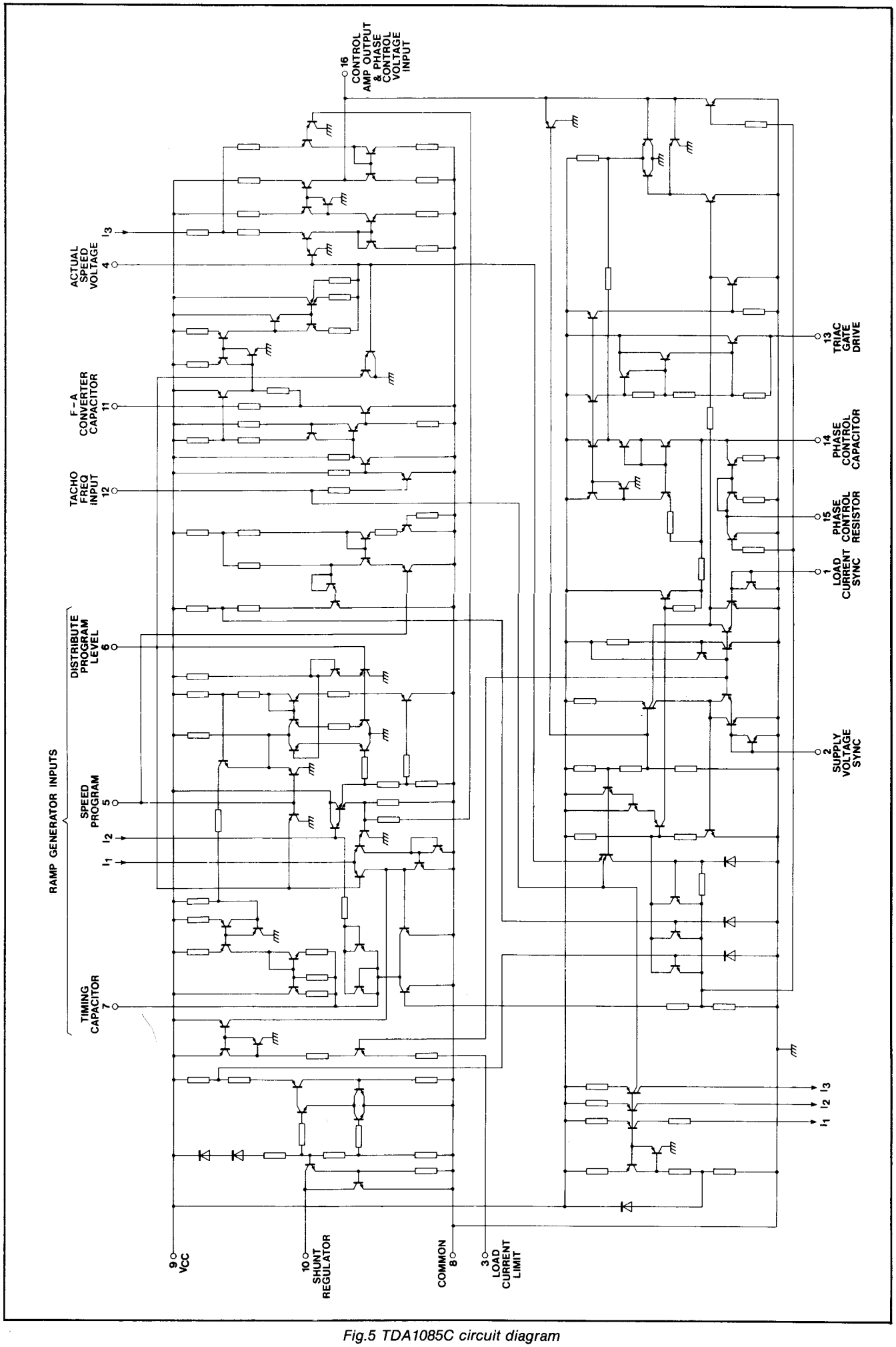
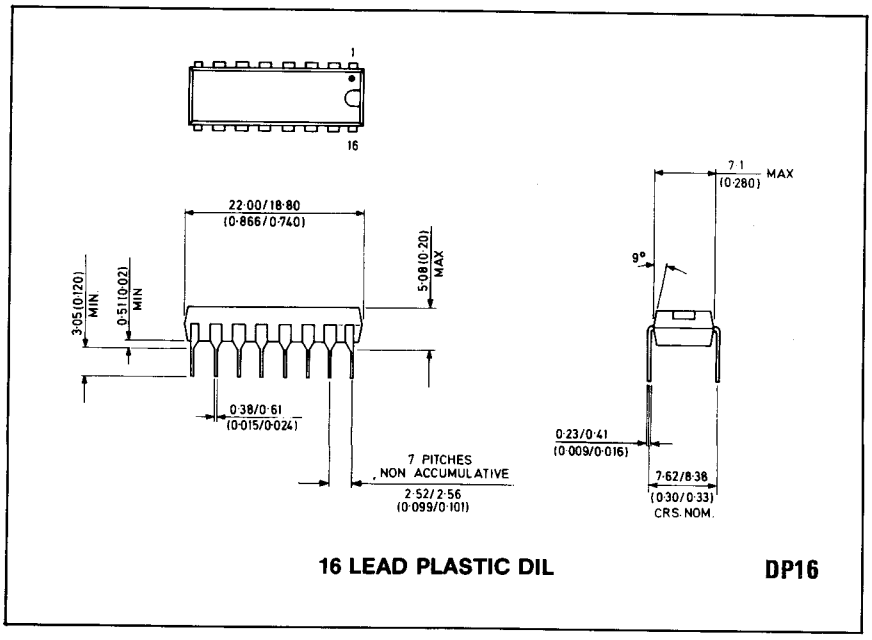


Fig.5 TDA1085C circuit diagram

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



16 LEAD PLASTIC DIL **DP16**

System Design

Throughout this section, component references are those shown on the Reference System Circuit Diagram, Fig.6.

ANALOGUE FEEDBACK CONTROL

An analogue feedback voltage (V_f) of OV to 13.5volts, may be supplied directly to pin 4. With this type of feedback the frequency-to-analog conversion circuit should be made inoperative by connecting pin 12 to common (pin 8).

Motor speed sensing can be achieved by rectifying and smoothing a tachogenerator signal, thus generating directly an analogue feedback control voltage. It is most important with this type of system that the tachogenerator does not pick up noise signals, particularly those generated by the motor field. This may well be a problem with simple tachos incorporated inside or close to the motor, but can easily be avoided by the use of digital sensing.

DIGITAL FEEDBACK CONTROL

In this type of feedback system the frequency of an input signal to pin 12 is converted to an analogue feedback control voltage (V_f). Although digital sensing requires an extra couple of passive components it offers the advantage of not requiring any calibration of the machine, plus stability against aging and temperature effects.

The zero voltage points of an AC tacho signal are sensed at pin 12.

Without diode D_2, the TDA1085C can function linearly with a range of tacho input signal levels between 0.2 and 6 volts. When D_2 is included, the device will function correctly, provided the positive tacho excursion does not exceed the open circuit tacho detection voltage (13.5 volts).

An over-voltage sensing circuit will reset the timing functions and inhibit triac drive pulses if the input exceeds 13.5 volts. Providing no resistive load is placed between pin 12 and common (pin 8), a 25μA tacho monitor bias current will cause the input pin voltage to exceed this limit if the tacho goes open circuit. By this means the TDA1085C is 'fail safe' in the event of tacho circuit failure.

Due to the inductive nature of a tacho pickup coil, the current output is proportional to the operating frequency. For a wide speed control range a predominantly frequency-independent voltage may be generated by integrating the pulses by means of a capacitor. C_3 performs this function; its value is dependent on the strength of the tacho signal.

Noise pickup by the tacho may be overcome by introducing an offset voltage (V_{to}) on the input. This is easily provided by R_9 and pin 12 bias current.

$$V_{to} = R_9 \times 25 \times 10^{-3} \text{ mV} \quad \ldots 1$$

R_9 also damps any resonance that may occur between C_3 and the tacho coil inductance.

Frequency to Analogue Conversion

The F-A converter may be used to transform the frequency derived from a tacho drive to an analogue voltage which is proportional to the motor speed. The tacho frequency is given by

$$f_t = \frac{SN}{120} \text{ Hz} \quad \ldots 2$$

Frequency to voltage conversion is achieved by integrating a pulse of charge (at pin 4) every time the tacho input (pin 12) goes positive. This unit of charge is defined by the capacitor connected to pin 11 (C_6) and is amplified by the circuit before being integrated at pin 4.

The conversion factor (K) is determined by C_6, R_{12} and the circuit gain (A_t), which may be calculated from

$$K = 10^3 (V_{cc} - 2V_{be}) A_t C_6 R_{12} \text{ mV/Hz} \quad \ldots 3$$

Simplifying gives

$$K \triangleq 14 \times 10^4 C_6 R_{12} \text{ mV/Hz} \quad \ldots 4$$

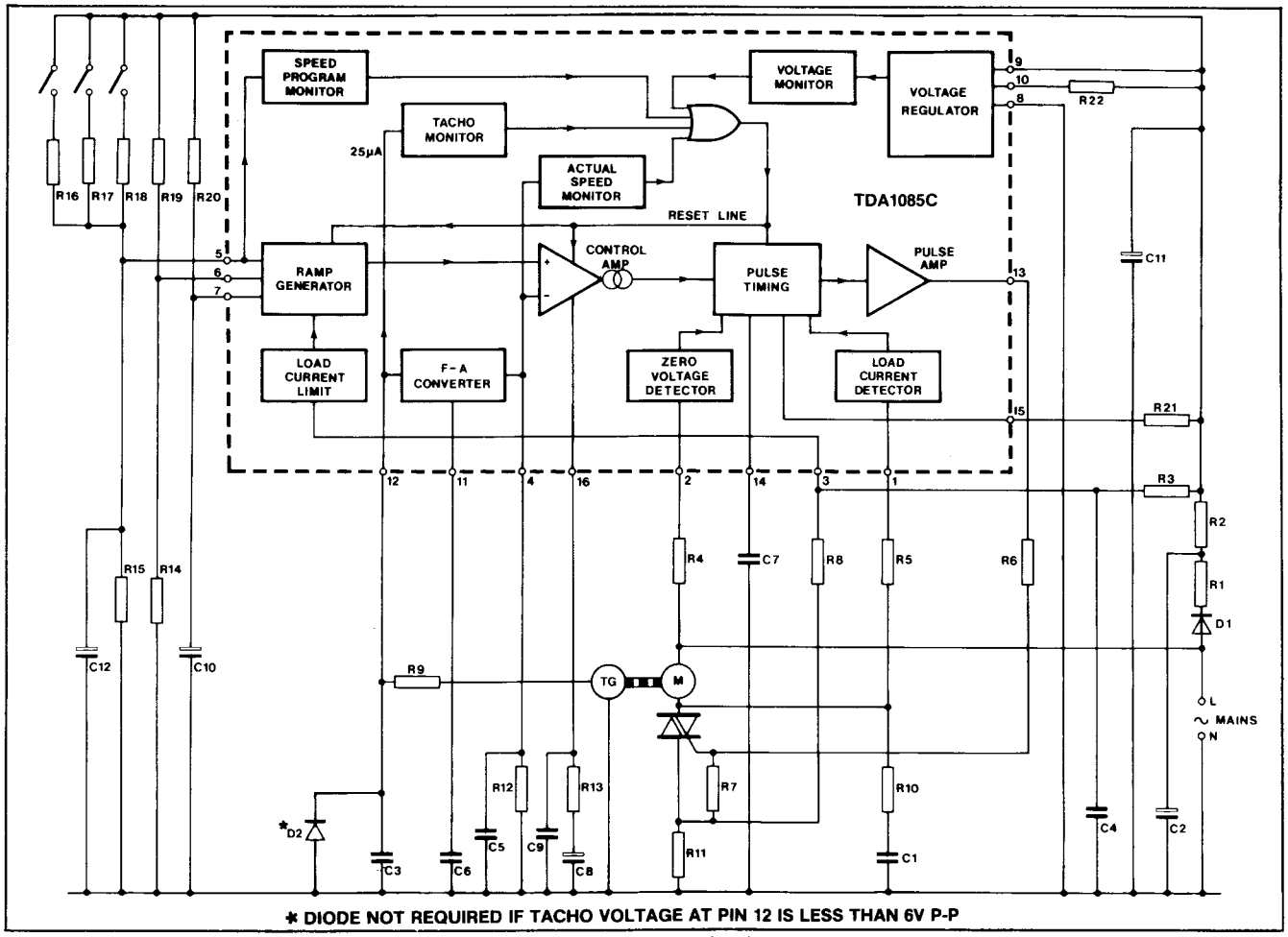
The analogue feedback voltage (V_f) generated by the converter circuit is hence given by

$$V_f = K f_t \times 10^{-3} \text{ volts} \quad \ldots 5$$

The maximum value of V_f which occurs at the highest motor speed should be designed to be $\leqslant$ 13.5volts.

During charge transfer the internal impedance of pin 11 is approximately 100kΩ, hence the time constant of the transfer period is $10^5 C_6$ seconds. This time constant should be designed to be a fraction of the minimum positive tacho input pulse duration, in order to maintain a linear relationship between the tacho frequency and the resulting tacho feedback voltage.

C_5 is used to integrate the pulses on pin 4. To maintain linear operation of the control amplifier the ripple voltage



* DIODE NOT REQUIRED IF TACHO VOLTAGE AT PIN 12 IS LESS THAN 6V P-P

Fig.6 Reference system circuit diagram

(V_{fr}) should be made less than 200mV. Increasing the value of C_5 will reduce the ripple but will also increase the response time of the F-A converter. The ripple voltage may be calculated from

$$V_{fr} = \frac{10^3 A_t (V_{cc} - 2V_{be}) C_6}{C_5} \text{ mV} \quad \ldots 6$$

Simplifying

$$V_{fr} \triangleq \frac{14 \times 10^4 C_6}{C_5} \text{ mV} \quad \ldots 7$$

The temperature coefficient and performance may be improved by incorporating a 470kΩ resistor from pin 11 to Vcc. This will affect the conversion factor since this resistor will be competing with the internal (100kΩ) impedance of pin 11, for current from C_6. Due to this and other component tolerances, it may be necessary to calibrate the system by means of a variable resistor on pin 4. These components are shown incorporated in Fig.13b.

Provided the tacho input voltage at pin 12 is kept below 6V p-p then diode D2 is not required. If the tacho input voltage exceeds this, then a 1N4148 Si diode should be used to clamp the negative excursion at pin 12.

THE RAMP GENERATOR

The ramp generator's function is to limit the rate of change of the speed reference voltage (V_s) applied to the control amplifier. Providing this is the slowest time constant in a system, the amplifier will remain in a linear proportional control mode and prevent an excessive phase angle (or power) being applied to the motor load.

A programmable slow ramp period is available to enable a 'distribution period' to be provided in automatic washing machines, i.e. a controlled slow acceleration period where clothes are distributed evenly around a revolving drum prior to spin.

The ramp generator is a follower integrator design, hence the internal ramp voltage will only rise to the voltage programmed on pin 5. Due to the circuit design the ramp voltage seen on pin 7, is a V_{be} higher than the internal level at which it is monitored. If the speed program voltage is increased (e.g. from 'wash' to 'spin') then the transition is again determined by the ramp generator characteristic between the two programmed levels. Also if the motor speed is restrained by an overload then the internal ramp voltage is restricted from exceeding the analogue feedback voltage (V_f) by more than V_{be}.

The fast ramp current (I_{rf}) is defined by the IC and is nominally 1.2mA. This current is integrated on pin 7 by C_{1o}, to produce a linear ramp. Assuming the current provided by R_{2o} is negligible compared to I_{rf}, the fast ramp rate (V_{rf}) is given by

$$V_{rf} = \frac{I_{rf}}{C_{1o}} \text{ mV/s} \quad \ldots 8$$

The knee voltages of the ramp (V_{ra} and V_{rb}) are dependent on the voltage programmed on pin 6 (V_6) (see Fig.3). These two levels define the speeds between which the motor will accelerate at the slow rate to provide a 'distribution period'. The relationships are

$$V_{rb} = 2V_6 \quad \ldots 9$$
$$\text{For } V_6 \leqslant 1.2V, V_{ra} = V_6 \quad \ldots 10$$
$$\text{For } V_6 \geqslant 1.2V, V_{ra} = 1.2V \quad \ldots 11$$

During the distribution period the ramp rate is predominantly defined by the current provided by R_{2o}. The average slow ramp rate (V_{rs}) may be calculated from

$$V_{rs} \triangleq \frac{2V_{cc} - 2V_{be} - V_{ra} - V_{rb}}{2R_{2o}C_{1o}} \times 10^3 \text{ mV/s} \quad \ldots 12$$

Simplifying gives

$$V_{rs} \triangleq \frac{30 - V_{ra} - V_{rb}}{2R_{2o}C_{1o}} \times 10^3 \text{ mV/s} \quad \ldots 13$$

The above expressions do not take account of the capacitor leakage current nor the residual charging current from pin 7. These parameters work against one another and therefore are self compensating to some extent. The leakage current of C_{1o} should be specified at a voltage equal to $V_{rb} + V_{be}$.

The distribution period (T_d) may be calculated from

$$T_d = \frac{V_{ra} - V_{rb}}{V_{rs}} \times 10^{-3} \text{ s} \quad \ldots 14$$

If a distribution period is not required, then pin 6 should be connected to common (pin 8). This circuit will then maintain a fast ramp up to the programmed speed voltage. A continuous slow ramp of exponential character can be provided by connecting pin 6 to pin 7. This maintains the circuit in a 'distribution' condition where the ramp is defined by R_{20} and C_{10}. Note that the bias current for pin 6 should be taken into account; it is expected to be less than $-10\mu A$ under these conditions.

SPEED PROGRAM VOLTAGE

The speed program voltage (V_s) on pin 5 must exceed the low threshold level of 80 mV. Timing functions will be reset and triac drive pulses will be inhibited if pin 5 is programmed below this level. The working range of V_5 is hence 80mV to 13.5 volts.

Pin 5 may be programmed by switching a resistor network to supply the required voltage levels. A small capacitor (C_{12}) may be required to prevent the ramp generator being reset due to pin 5 input going momentarily low.

THE CONTROL AMPLIFIER

The differential control amplifier is normally used to compare the analogue feedback voltage (V_f), pin 4, with the internal speed reference voltage (V_s) and hence derive a phase control voltage (V_p) on pin 16. The amplifier has a transconductance gain of $300\mu A/V$ with a limited bidirectional output drive capability of $\pm 100\mu A$. Hence proportional control occurs for a differential error input of ± 330mV.

The gain and phase compensation for closed loop control systems are determined by R_{13}, C_8 and C_9 connected to pin 16. These components are best chosen empirically to achieve a best compromise in terms of speed overshoot and response time.

For manual or open loop phase control, the control amplifier may be used as a buffer amplifier and use made of the ramp generator to control the rate of phase angle increase. This may be accomplished by connecting pin 4 to pin 16, grounding pin 12 to pin 8 and controlling the phase angle via the voltage applied to pin 5.

The maximum phase angle may be limited in both open and closed loop control systems by clamping the maximum voltage on pin 16 by means of a zener diode or other clamping device. Since there is only $100\mu A$ current drive from the control amplifier, it is important that the clamping device or circuit has a sharp turn-on knee.

During a reset condition pin 16 will be pulled low, ensuring that no output pulses are generated. When the inhibit signal is removed the phase angle increases from zero conduction at a controlled rate.

ZERO VOLTAGE DETECTOR

The sole purpose of the zero voltage detector is to reset the ramp generator of the pulse timing circuit at the zero voltage point of the mains cycle.

The AC mains is applied, via R_4, to a synchronisation circuit (pin 2) which produces a reset pulse whenever the input current is between $\pm 50\mu A$. The pulse is symmetrical around the zero voltage points, which ensures that positive and negative wave triac conduction symmetry can be obtained.

R_4 should be chosen to limit the peak current drive to pin 2 to be slightly less than ± 1mA.

LOAD CURRENT DETECTOR

The load current detector inhibits triac gate pulses being generated by the pulse timing circuit until correct conditions exist for the triac to latch when fired. This condition exists when there is sufficient voltage across the triac to induce the required latching current within the duration of a firing pulse.

The triac voltage is monitored by means of R_5 in a similar manner to the zero voltage detector. In this case triac gate pulses are inhibited if the current into pin 1 is not greater than $\pm 50\mu A$. Again the peak current drive should not exceed ± 1mA. From the above it follows that the minimum voltage across the triac when a gate pulse is supplied is given by

$$V_{tx} = R_5 \times 50 \times 10^{-6} \text{ volts} \quad \ldots 15$$

TRIAC PULSE TIMING

The function of the pulse timing circuit is to control the delay and duration of the triac firing pulse. The pulse position is determined by resetting the ramp generator at the mains zero voltage points and triggering the pulse generating circuit when the ramp reaches a level determined by the phase angle control voltage on pin 16. With inductive loads the pulse may be further delayed by the load current detector circuit.

Full power may be supplied to inductive loads since when maximum conduction is demanded the triac pulse is delayed until the lagging load current from the previous half cycle has reduced to zero. At this point the triac will cease to conduct and the supply voltage will appear across it, which when detected initiates the next triac pulse.

At high motor speeds brush bounce may become severe and cause interruptions of the motor load current. Under these conditions the load current detector will respond to the supply voltage appearing across the triac and hence enable a retriggering pulse to be supplied.

The ramp waveform is generated by charging capacitor C_7 up to 12.8volts (nominal) during the zero voltage pulse determined by the zero voltage detector (pin 2). The charging current in this period is limited by an internal impedance of approximately 500ohms. After the zero voltage pulse, C_7 is discharged in a linear fashion by a current sink (I_d), defined externally on pin 15. When the voltage on C_7 reaches a value determined by the phase control voltage on pin 16 a triac gate pulse is initiated. The dynamic working range of this ramp generator is 11.7volts, i.e. the triac gate pulse may be created at any time before the ramp waveform has decreased by this voltage.

The triac pulse duration is determined by recharging C_7 with an internally defined current (I_r) to a voltage 100mV (nominal) above the original trip voltage. During this period the discharge current (I_d) is maintained and hence works against the charging current (I_r). Therefore, I_d must be smaller than I_r for the circuit to function as a pulse generator.

If retriggering occurs, the minimum delay will be determined by the time taken for the current I_d to discharge C_7 back to the original trip voltage i.e. back through 100mV. The maximum retriggering rate (t_r) is thus determined by this delay time plus the pulse duration.

Triac Pulse Timing Equations

Ramp discharge current

$$I_d = \frac{(V_{cc} - V_{be})}{R_{21}} \times 10^6 \ \mu A \quad \ldots 16$$

Dynamic ramp voltage on pin 14

$$V_{rp} = \frac{I_d \times 10^{-6}}{2 \times f_m \times C_7} \text{ Volts} \quad \ldots 17$$

Limitation on V_{rp} for full phase control

$$V_{rp} < 11.7 \text{ Volts} \quad \ldots 18$$

TRIAC GATE PULSE

A triac pulse width of 50μs is suitable for most general purpose triacs. Standard component values for C_7 and R_{21} may hence be used which are as follows:

For 50 Hz supply

$C_7 = 47\,nF \pm 10\%$
$R_{21} = 300\,k\Omega \pm 5\%$

For 60 Hz supply

$C_7 = 47\,nF \pm 10\%$
$R_{21} = 270\,k\Omega \pm 5\%$

With the above components the retriggering period will be approximately 200μs

TRIAC GATE DRIVE

The triac gate pulse is amplified by a buffer amplifier that provides a positive low impedance emitter follower output drive to pin 13.

The current drive required will depend on the characteristics of the triac used. It is important to provide sufficient gate current to guarantee complete bulk conduction is achieved; if not, hot spots may occur which will reduce the life of the triac. The worst case condition is likely to exist when the device is fired in the fourth quadrant (i.e. positive current drive into the gate when a negative voltage is present on Main Terminal 2 (MT2) of the triac).

With sensitive triacs, R_7 may be required to provide a path for the output leakage current and make the triac less susceptible to false triggering from electrical noise.

The triac gate current drive may be calculated from

$$I_{tg} = \frac{V_{13} - V_{tg}}{R_6} - \frac{V_{tg}}{R_7} \times 10^3\ mA \qquad \ldots 19$$

TRIAC LATCHING

As mentioned before, it is necessary to trigger the triac when conditions are right for a latching current to be established within the period of the gate pulse.

When switching on an inductive load the initial current will increase from zero at a rate dependent on the voltage across and the inductance of the load (the minimum voltage being determined by the load current detector). To help with latching, additional triac load current for a short duration can be provided if required by means of a series RC network in parallel with the triac. C_1 and R_{10} provide this function as well as offering some protection from dv/dt triggering of the triac due to noise spikes on the mains.

OVERLOAD CURRENT PROTECTION

The purpose of motor current limitation is more to protect the triac than the motor itself. Since the stall current is generally much higher than that required for maximum working torque, a limitation can be set at a lower value thus guaranteeing safe operation of the triac under all load conditions.

Peak load current limiting can be provided by discharging the ramp generator capacitor (pin 7) with a current that is proportional to the current drawn from pin 3, when the trip threshold is exceeded. This reduces the internal speed reference voltage (V_s) to a level such that a reduction in phase angle conduction is made, hence reducing the load current. The current limit input is a common base transistor which conducts when the emitter, connected to pin 3, is driven negatively with respect to common (pin 8). The current gain (A_{il}) is the ratio of the discharge current from pin 7 to the current drawn from pin 3.

Load current is monitored by means of a low value resistor (R_{11}) connected in series with the load. The voltage developed across this resistor drives the current limit circuit via resistors R_3 and R_8, such that the voltage on pin 3 is zero at the desired peak load current. The sensitivity of the circuit (i.e. the rate at which the circuit reacts to over-current) will depend on the drive impedance, this being predominantly determined by the resistance of R_8. With a circuit as shown in the reference circuit diagram the load current is monitored in the negative supply cycle.

The value of R_{11} is normally chosen such that a fraction of a volt is generated across it, thus minimising power dissipation yet providing a reasonable signal to drive the overload current circuit. The peak load current is determined by

$$I_{pl} = \frac{V_{cc}}{R_{11}} \times \frac{R_8}{R_3}\ A \qquad \ldots 20$$

High frequency noise may be generated by short duration changes in load current produced by commutator action in a motor load. Due to the low impedance required R_{11} will normally be a wire wound resistor and hence have some inductance, which will increase the noise voltage driving into pin 3. This can be filtered by the inclusion of capacitor C_4.

If overload current limiting is not required, pin 3 should be left open circuit.

CURRENT CONSUMPTION

The total supply current required can be calculated from the sum of the following:

I IC operating current

This is the current required by the circuit which is not dependent on external circuitry.

$$i_I = 7.4\,mA \pm 20\% \qquad \ldots 21$$

II Slow ramp generator current

This is usually very small and may be neglected. If required it may be calculated from:-

$$i_{II} = \frac{V_{CC}}{R_{20}} \times 10^3\ mA \qquad \ldots 22$$

III Frequency to analogue conversion current

This is the additional dynamic operating current required. Again this is usually negligible but may be calculated from:-

$$i_{III} = f_t\,(V_{cc} - 2V_{be})\,C_{11}\,(1 + A_t) \times 10^3\ mA \qquad \ldots 23$$

IV Voltage and current synchronisation currents

The AC input currents to pins 1 & 2 cause a drain from the positive sypply, the additional current required is given by:-

$$i_{IV} = \frac{\sqrt{2}\,V_{AC}}{\pi}\left(\frac{1}{R_4} + \frac{1}{R_5}\right)10^3\ mA \qquad \ldots 24$$

V Pulse timing current

This is the dynamic operating current of the pulse timing circuit which is determined by the current fed into pin 15. Normally this current is small and has little effect on the total current required.

$$i_V = \frac{2(V_{cc} - V_{be})}{R_{21}} \times 10^3\ mA \qquad \ldots 25$$

VI Triac gate current

The average triac gate drive current may be calculated from

$$i_{VI} = 2f_m \cdot x\ t_p\ x\ I_{tg}\ (1 + P_t)\ x\ 10^{-6}\ mA \qquad \ldots 26$$

The probability factor P_t has been incorporated to take account of current required for additional triac pulses. These will only be required if the load current is interrupted, for example by motor brush bounce.

VII Other external circuitry

Regulated supply current may also be required for biasing control inputs to pins 5 and 7 and other auxilliary circuitry.

When a reset condition exists the IC operating current increases by a maximum of 1 mA. This will occur when the

supply is being established hence this current needs to be catered for. However during a reset condition no triac pulses will be generated, therefore only the greater of these two currents needs to be provided.

When calculating the supply current required, the worst case conditions (i.e. component tolerance etc) should be incorporated in the above equations.

$$I_s = \Sigma i \qquad \ldots 27$$

VOLTAGE REGULATOR CIRCUIT

A shunt type voltage regulator circuit is incorporated in the circuit to maintain a steady positive supply on pin 9. Ths enables the device to be driven direct from the mains via current limiting and smoothing components. Since the current shunt (pin 10) is not directly connected to the positive supply (pin 9) it is also possible to power the circuit direct from a DC supply or use pin 10 to drive a series regulating transistor as shown in Fig.7.

A voltage monitor circuit senses the voltage on pin 9 (V_{cc}), this inhibits triac firing pulses and resets the timing functions until an adequate supply for correct circuit operation has been established. Hysteresis in the monitor circuit gives rise to two trip levels, namely the enable (V_{me}) and disable (V_{md}) voltages.

Where use is made of the shunt regulator, unwanted current is drained by pin 10 to common. Power dissipation by the device can be minimised by incorporating resistor R_{22}, enabling greater supply currents to be regulated. Under worst case conditions it is important that the voltage dropped across this resistor does not exceed 13volts.

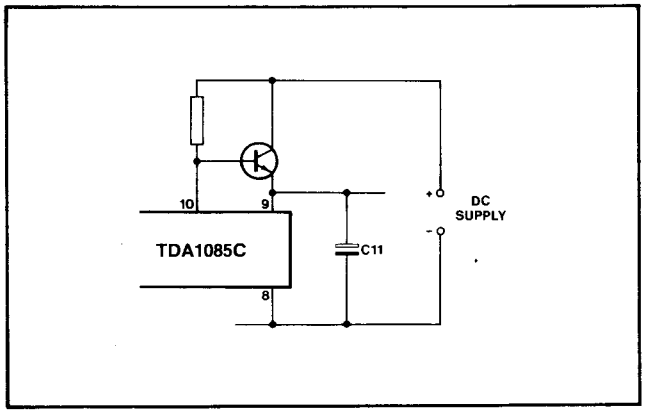


Fig.7 Series regulated DC supply

AC SUPPLY CIRCUITS

The simplest AC supply circuit is shown in Fig.8. This circuit will produce ripple on the regulated supply (pin 9) and will hence cause some asymmetry in firing between positive and negative cycles of the mains. Component values may be calculated from:

$$C_{11} = \frac{I_s}{V_{cr} \times f_m} \times 10^3\ \mu F \qquad \ldots 28$$

$$R_1 = \frac{\frac{\sqrt{2}}{\pi} V_{ac} - V_{cc}}{I_s(mA)} \times 10^3 \text{ ohms} \qquad \ldots 29$$

$$P_{dr} = \frac{(\sqrt{2}\,V_{ac} - V_{cc})^2}{4R_1} \text{ Watts} \qquad \ldots 30$$

Where it is important to provide symmetrical firing, further filtering of the AC supply will be required as shown in Fig. 9. Although additional components are required the total capacitance is less than that required in the simple circuit.

The circuit should be designed such that the half wave rectified current is roughly smoothed by capacitor C_2. R_2 and C_2 are chosen such that they are capable of maintaining the average current required by the circuit (I_s). The peak demands during triac gate pulses are then

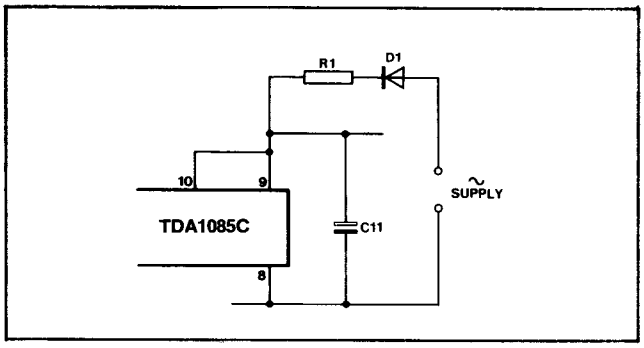


Fig.8 Simple shunt regulated supply

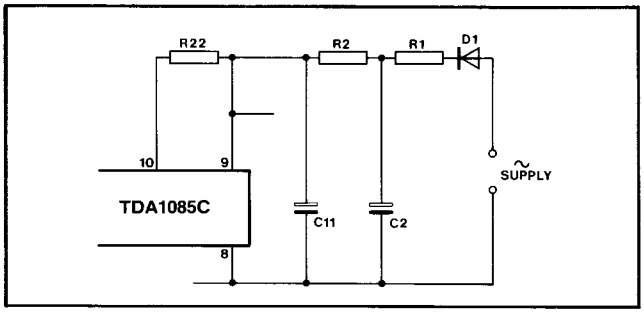


Fig.9 Resistive feed shunt regulated to provide a low ripple supply

catered for by capacitor C_{11}. The dropper resistors may be calculated from:

$$R_1 + R_2 = \frac{\frac{\sqrt{2}}{\pi} V_{ac} - V_{cc}}{I_s(mA)} \times 10^3 \text{ ohms} \qquad \ldots 31$$

$$P_{dr} = \frac{(\sqrt{2}V_{ac} - V_{cc} - I_s R_2)^2}{4R_1} \text{Watts} \qquad \ldots 32$$

Where power dissipation is a problem the circuit may be powered by a reactive feed from the AC supply as shown in Fig. 8. Resistor R_x should be included to limit current due to noise spikes from the supply. An impedance of the order of 200ohms is suitable for this purpose. Neglecting the effects of this resistor, the value of capacitor C_x may be calculated from:-

$$C_x = \frac{I_s}{f_m(2\sqrt{2}V_{ac} - I_s R_2 - V_{cc})} \times 10^3 \mu F \qquad \ldots 33$$

NB *Worst case conditions should be put in the above equations when calculating component values etc.*

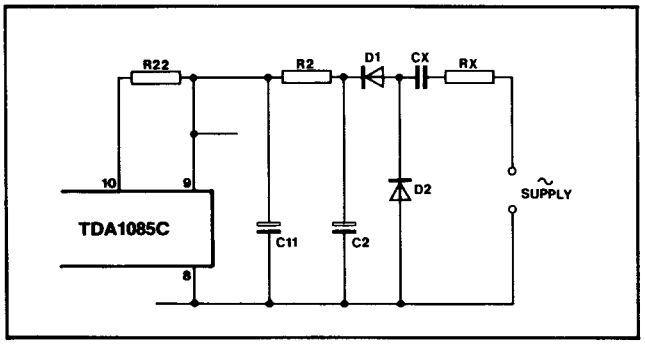


Fig.10 Reactive feed shunt regulated to provide a low ripple supply with minimum power dissipation

TRIAC LATCHING CIRCUIT

When driving inductive loads a series RC network may be required across the triac. This is to provide a short duration load current in the triac while the current in the main inductive load is being established after a gate pulse is applied. In this way a latching current can be quickly established, even when the triac is fired at low voltage points in the mains cycle. C_1 and R_{10} provide this function as shown in Fig.6.

SYMBOLS USED IN TEXT

Symbol	Function	Units
A_{il}	Current limit gain	—
A_t	IC tacho conversion gain	—
f_m	Mains frequency	Hz
f_f	Tacho frequency	Hz
I_d	Pulse ramp discharge current	μA
I_r	Pulse ramp recharge current	μA
I_{rf}	Fast ramp current	mA
I_s	Supply current	mA
I_{fg}	Peak triac gate current	mA
K	Tacho conversion factor	mV/Hz
N	Number of tacho poles	—
P_{dr}	Power dissipation by dropper resistor (R1)	Watts
P_t	Probability of extra triac pulse	—
S	Motor speed	RPM
t_d	Distribution period	seconds
t_p	Pulse duration	μs
t_r	Pulse retriggering rate	μs
V_{ac}	AC supply voltage (RMS)	volts
V_{be}	Transistor emitter base voltage	volts
V_{cc}	Positive rail voltage (pin 9)	volts
V_{cr}	Supply ripple voltage	volts
V_f	Analog feedback voltage	volts
V_{fr}	Feedback voltage ripple (pk—pk)	mV
V_{me}	Voltage monitor enable level	volts
V_{md}	Voltage monitor disable level	volts
V_p	Phase control voltage	volts
V_{ra}	Ramp voltage at first knee	volts
V_{rb}	Ramp voltage at second knee	volts
V_{rf}	Fast ramp rate	mV/s
V_{rp}	Dynamic ramp voltage	volts
V_{rs}	Slow ramp rate	mV/s
V_s	Internal speed reference voltage	volts
V_{tg}	Triac gate voltage	volts
V_{fo}	Tacho offset voltage	mV
V_{fx}	Voltage across triac	volts
V_5	Speed program voltage on pin 5	volts
V_6	Distribution level programmed on pin 6	volts
V_{13}	Pulse drive voltage from pin 13	volts

Motor Control Applications

THE UNIVERSAL MOTOR

This is a machine which has a commutator drive to the armature and a field that is polarised by the supply. The field and armature may be series or parallel connected such that the machine in principle could be driven from a DC or AC supply. Most domestic type motors are series connected.

In controlling this type of machine, the phase angle may be varied from zero to a maximum determined by the lag in load current due to inductance. To obtain full power it is therefore necessary to have a load current detection circuit such that the triac is not fired before the current from the previous half cycle has reduced to zero.

At high motor speeds brush bounce may also be a problem. This can cause an interruption in load current and hence unlatch the triac, reducing the power to the motor. To overcome this problem it is necessary to detect the situation and retrigger the triac.

Both these problems are overcome in the TDA1085C circuit by means of the load current synchronisation circuit (pin 1).

THE FIXED FIELD MOTOR

This is a machine which has a constant field which may be provided by permanent magnets in the stator. The armature requires a DC supply to drive the motor, and hence this may be said to be a DC machine.

This type of motor may be driven from an AC supply by means of a rectifying circuit. The machine will generate a back EMF that is proportional to its speed and will therefore only draw load current when the supply voltage is greater than the generated EMF.

When driving this type of load with a phase control circuit the triac cannot be latched before a 90° phase angle since the EMF generated will be almost equal to the peak supply voltage from previous cycles, and hence no load current will flow until the peak supply voltage is reached again. For this reason it is desirable to be able to limit the triac gate pulse to the second half of each half cycle of the supply. With the TDA1085C the maximum conduction angle may be limited by restricting the voltage on pin 16 by means of a zener diode.

Since load current only follows for a short period of each half cycle a high peak current is to be expected. This, if unchecked, may cause damage to the triac and rectifying devices. By incorporating an inductor in series with the motor, the load current may be controlled in its build-up rate and spread over a greater period, hence reducing its peak value for a particular load demand.

THE INDUCTION MOTOR

The principle of an induction motor is to generate a rotating magnetic field in which the rotor is placed. Due to the generation of eddy currents the rotor will react and follow the field. The difference between the field and rotor speeds is known as the slip speed which increases with applied load.

The main disadvantage of this type of machine is that it has a poor torque speed characteristic which makes it unsuitable for variable speed applications where a high torque is required at low speeds. They may however, be suitable for driving loads such as fans or centrifugal pumps where the load torque reduces with decreasing speed.

Due to the high inductance of this type of machine a poor load power factor results. This may be improved by running the motor at a fixed slip speed by the use of a phase control circuit. A significant saving in real power consumed will also be obtained when the motor is lightly loaded.

When using phase control with this type of motor it is most important that symmetrical firing of the positive and negative waves is achieved otherwise a small net DC voltage may generate a high DC current in the stator windings. The TDA1085A is capable of meeting this requirement.

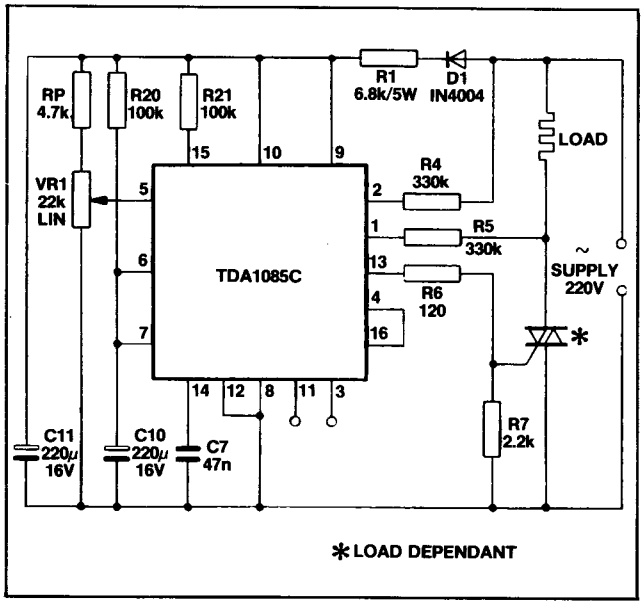


Fig.11 Manual phase control circuit

MANUAL PHASE CONTROL CIRCUIT

Fig.11 shows an open loop phase control circuit using the ramp generator of the TDA1085C to limit the rate of increase of the phase angle. R_{20} and C_{10} give a time constant of 22 seconds.

UNIVERSAL MOTOR APPLICATION

The circuit of Fig. 11 is essentially the same as the reference circuit Fig. 4, but with component values added. The specification is as follows:

Supply:	220V ± 15% 58Hz
Motor:	Normal load current 7A RMS
	Peak load current limit 21A
Tacho:	8 poles
	Amplitude at max. speed 14V RMS
Motor speed requirements	Wash speed 800RPM
	Distribute speeds 600 to 1200RPM
	Spin speeds 5,000RPM
	Super spin speeds 10,000RPM
Distribution time:	20 seconds

FIXED FIELD MOTOR APPLICATION CIRCUIT

Specification for the circuit shown in Fig. 10:

Supply:	220V ± 15% 50Hz
Motor:	Peak load current limit 30A
Tacho:	8 poles
	Amplitude at maximum speed 14V RMS
Motor speed:	Variable up to 10,000 RPM

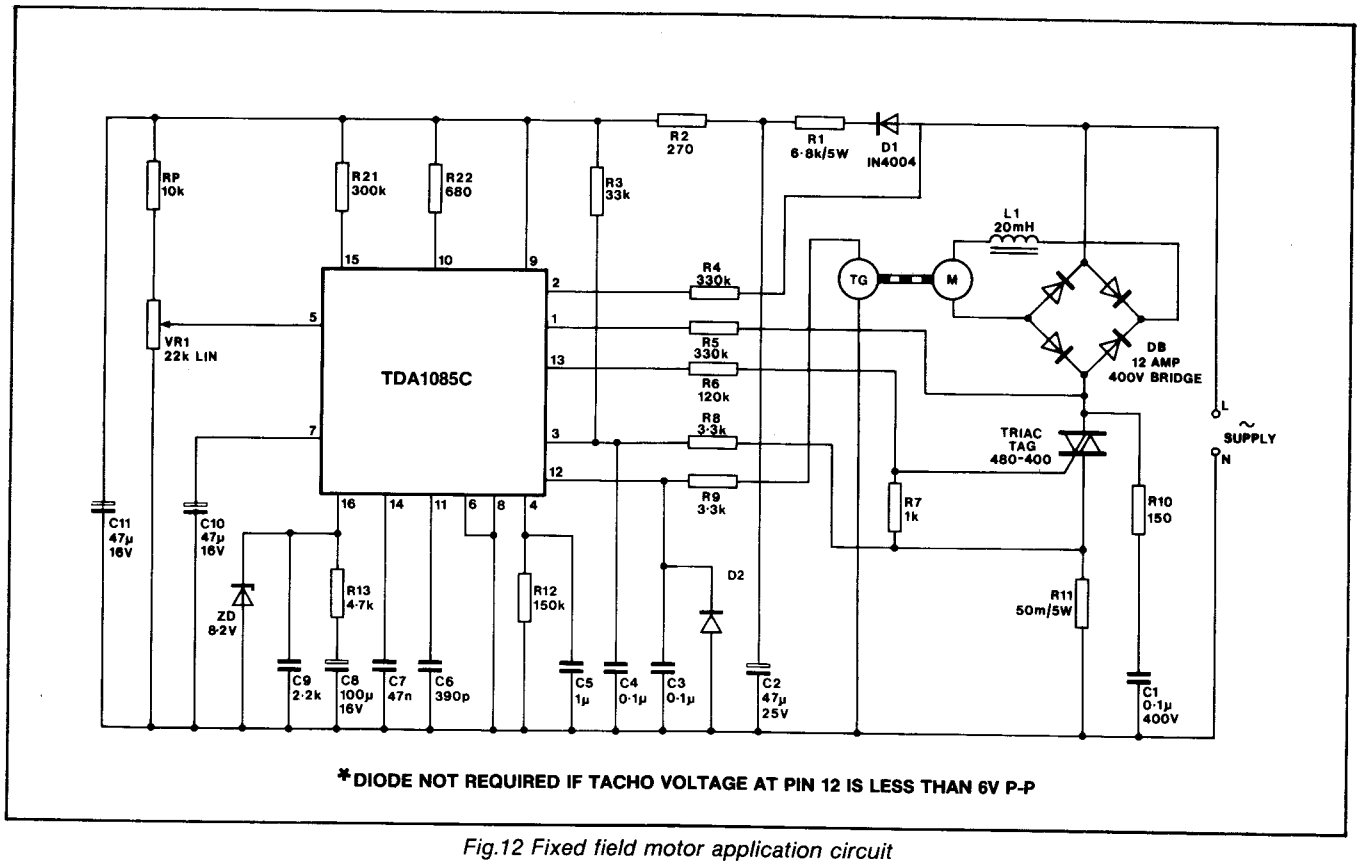


Fig.12 Fixed field motor application circuit

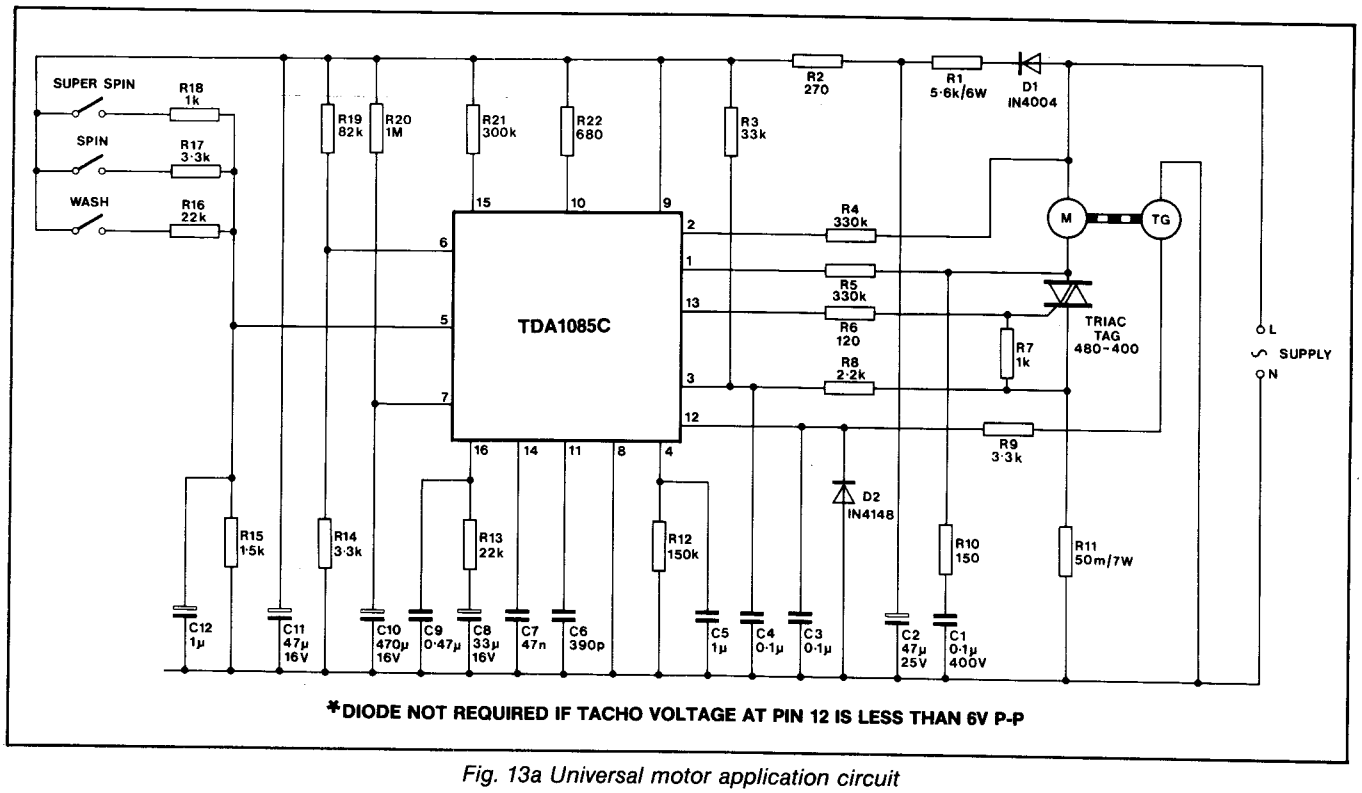


Fig. 13a Universal motor application circuit

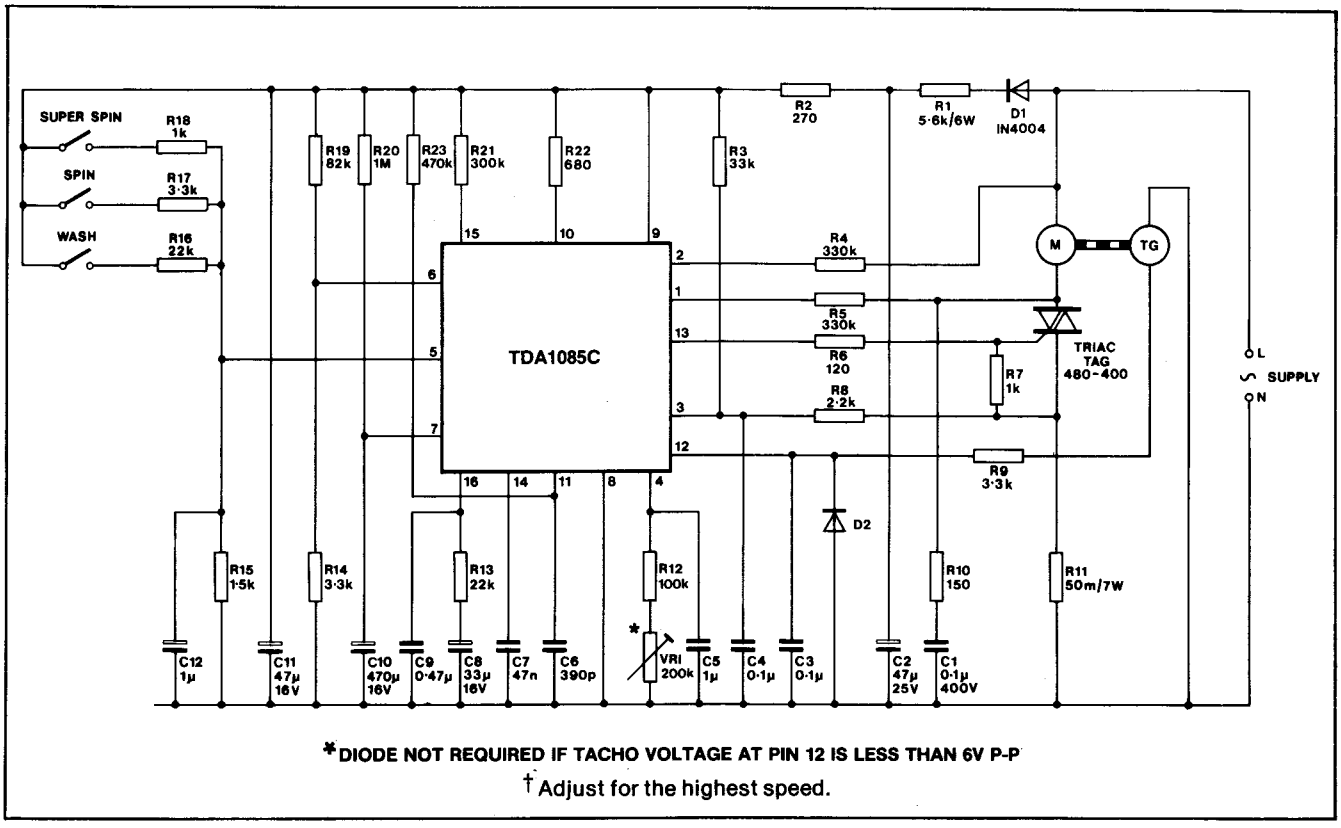


Fig.13b Calibrated universal motor application circuit