



TDA1670A

# LINEAR INTEGRATED CIRCUITS

## PRELIMINARY DATA

### VERTICAL DEFLECTION CIRCUIT

The TDA 1670A is a monolithic integrated circuit in 15-lead Multiwatt<sup>®</sup> package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110° colour TV picture tubes. It offers a wide range of applications also in portable CTVs, BW TVs, monitors and displays. The functions incorporated are.

- Synchronization circuit
- Precision oscillator and ramp generator
- Power output amplifier with high current capability
- Flyback generator
- Voltage regulator
- Precision blanking pulse generator
- Thermal shut down protection
- CRT screen protection circuit which blanks the beam current in the event of loss of vertical deflection current.

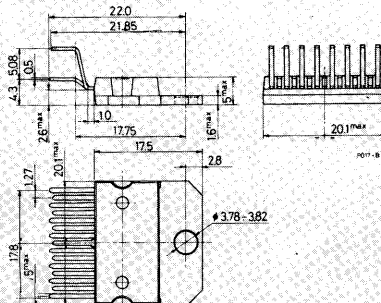
### ABSOLUTE MAXIMUM RATINGS

$V_s$	Supply voltage at pin 14	35	V
$V_1, V_2$	Flyback peak voltage	60	V
$V_5$	Sync. input voltage	20	V
$V_{11}, V_{12}$	Power amplifier input voltage	$\begin{cases} V_s \\ -10 \end{cases}$	V
$V_{13}$	Voltage at pin 13	$V_s$	
$I_o$	Output current (non repetitive) at $t = 2$ msec	3	A
$I_o$	Output peak current at $f = 50$ Hz $t > 10 \mu\text{sec}$	2	A
$I_o$	Output peak current at $f = 50$ Hz $t \leq 10 \mu\text{sec}$	3.5	A
$I_{15}$	Pin 15 peak to peak flyback current at $f = 50$ Hz, $t_{fly} \leq 1.5$ msec	3	A
$I_{15}$	Pin 15 DC current at $V_1 < V_{14}$	100	mA
$P_{tot}$	Maximum power dissipation at $T_{case} \leq 60^\circ\text{C}$	30	W
$T_{stg}, T_j$	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

ORDERING NUMBER: TDA 1670A

### MECHANICAL DATA

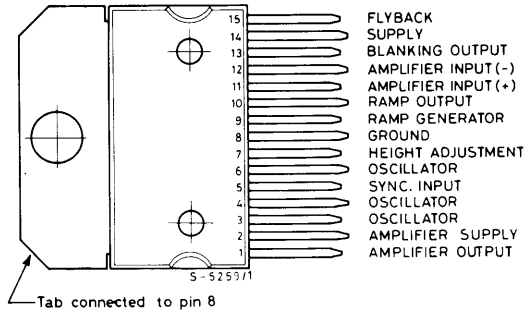
Dimensions in mm



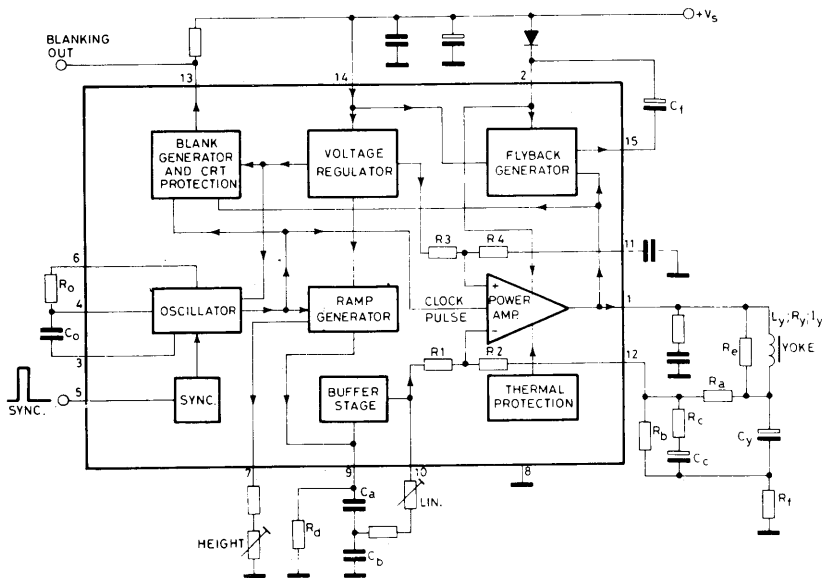


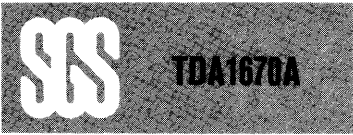
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### CONNECTION DIAGRAM (top view)

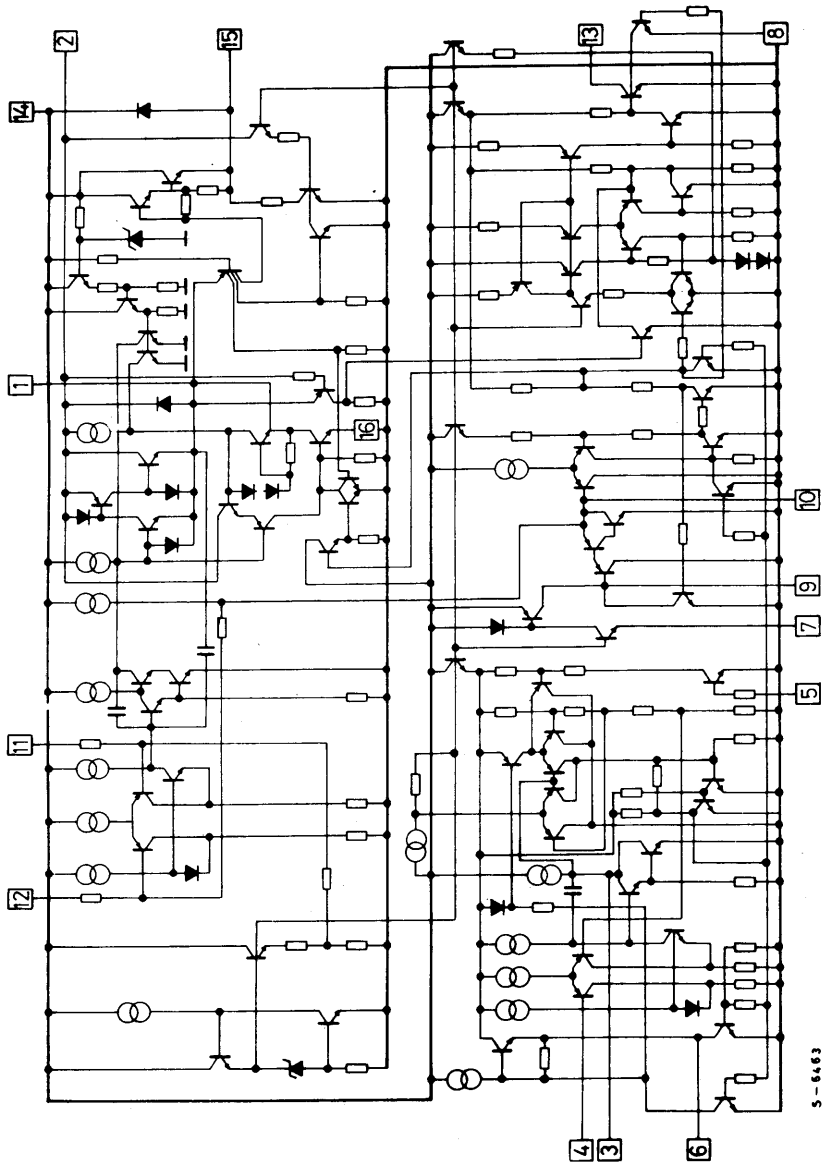


### BLOCK DIAGRAM





SCHEMATIC DIAGRAM



5-6463



**THERMAL DATA**

$R_{th\ j-case}$	Thermal resistance junction-case	max	3	°C/W
$R_{th\ j-amb}$	Thermal resistance junction-ambient	max	40	°C/W

**ELECTRICAL CHARACTERISTICS** ( $V_s = 35V$ ,  $T_{amb} = 25^\circ C$ , unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	Fig.
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**DC CHARACTERISTICS**

$I_2$	Pin 2 quiescent current	$I_1 = 0$		16	36	mA	1b
$-I_9$	Ramp generator bias current	$V_9 = 0$		0.02	1	$\mu A$	1b
$-I_9$	Ramp generator current	$V_9 = 0$ ; $-I_7 = 20\ \mu A$	18.5	20	21.5	$\mu A$	1b
$\left  \frac{\Delta I_9}{I_9} \right $	Ramp generator non linearity	$\Delta V_9 = 0$ to $15V$ $-I_7 = 20\ \mu A$		0.2	1	%	1b
$I_{14}$	Pin 14 quiescent current			25	45	mA	1b
$V_1$	Quiescent output voltage	$V_s = 35V$ ; $R_a = 2.2\ K\Omega$ $R_b = 1\ K\Omega$	16.4	17.8	19.5	V	1a
		$V_s = 15V$ ; $R_a = 390\Omega$ $R_b = 1\ K\Omega$	6.9	7.5	8.1	V	
$V_{1L}$	Output saturation voltage to ground	$I_1 = 1.2A$		1	1.4	V	1c
$V_{1H}$	Output saturation voltage to supply	$-I_1 = 1.2A$		1.6	2.2	V	1d
$V_4$	Oscillator virtual ground			0.45		V	1b
$V_7$	Regulated voltage at pin 7	$-I_7 = 20\ \mu A$	6.3	6.6	7	V	1b
$\frac{\Delta V_7}{\Delta V_s}$	Regulated voltage drift with supply voltage	$\Delta V_s = 15$ to $35V$		1	2	$\frac{mV}{V}$	1b
$V_{11}$	Amplifier input (+) reference voltage		4.1	4.4	4.7	V	1b
$V_{13}$	Blanking output saturation voltage	$I_{13} = 10\ mA$		0.35	0.5	V	1a
$V_{15}$	Pin 15 saturation voltage to ground	$I_{15} = 20\ mA$		1	1.5	V	1a

Fig. 1 - DC test circuit

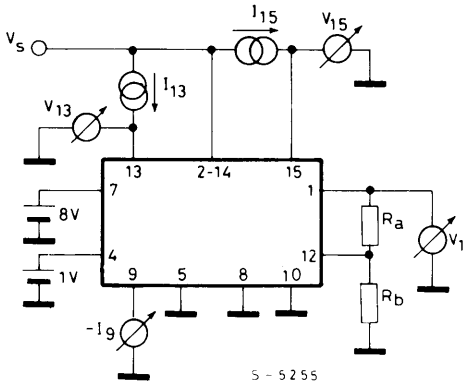


Fig. 1a

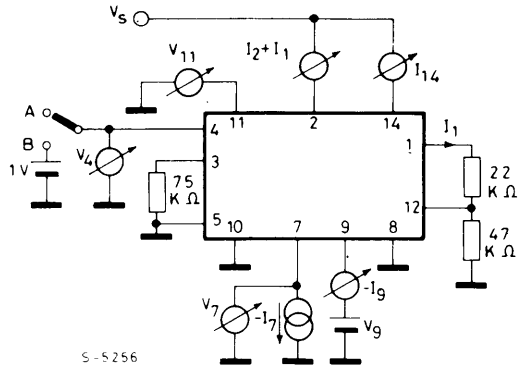


Fig. 1b

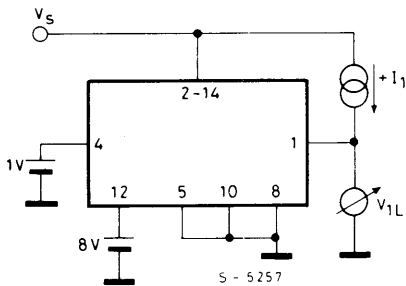


Fig. 1c

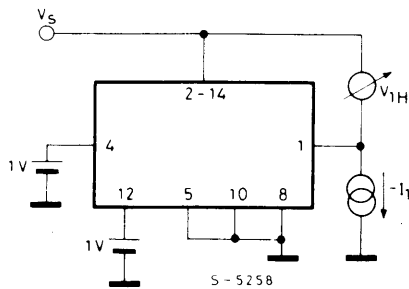
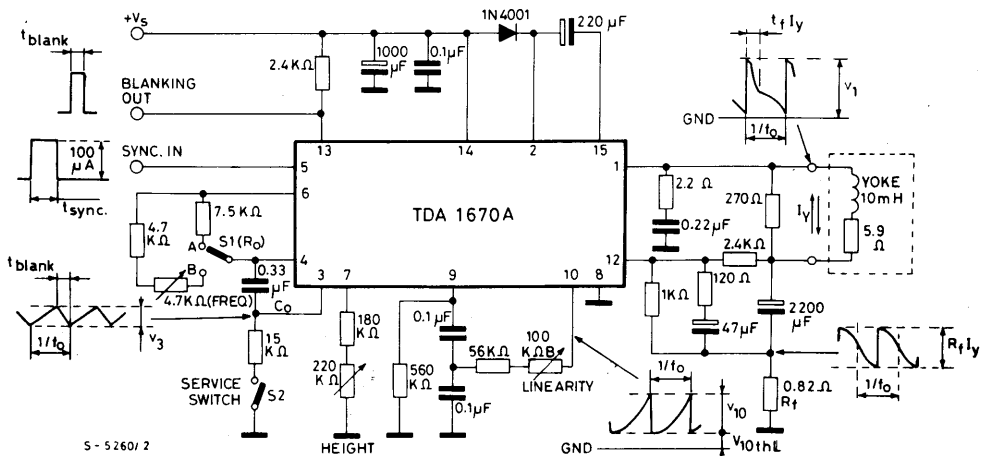


Fig. 1d

**ELECTRICAL CHARACTERISTICS** (Refer to the A.C. test circuit of fig. 2,  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_s = 24\text{V}$ ,  $f = 50\text{ Hz}$ , unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$I_s$	Supply current	$I_y = 2\text{ App}$	295		mA	
$I_5$	Sync input current required to sync.		100		$\mu\text{A}$	
$V_1$	Flyback voltage	$I_y = 2\text{ App}$	50		V	
$V_3$	Peak to peak oscillator sawtooth voltage	$I_5 = 0$	3.6		V	
		$I_5 = 100\ \mu\text{A}$	3.4		V	
$V_{10thL}$	Start scan level of the input ramp		1.85		V	
$t_{fly}$	Flyback time	$I_y = 2\text{ App}$	0.6		ms	
$t_{blank}$	Blanking pulse duration	$f_o = 50\text{ Hz}$ $T_j = 75^{\circ}\text{C}$	1.33	1.4	1.47	ms
		$f_o = 60\text{ Hz}$ $T_j = 75^{\circ}\text{C}$		1.17		ms
$f_o$	Free running frequency	$R_o = 7.5\text{ K}\Omega$ $C_o = 330\text{ nF}$ $T_j = 75^{\circ}\text{C}$	42	43.5	45	Hz
		$R_o = 6.2\text{ K}\Omega$ $C_o = 330\text{ nF}$ $T_j = 75^{\circ}\text{C}$		52.5		Hz
$\Delta f$	Synchronization range	$I_5 = 100\ \mu\text{A}$ $T_j = 75^{\circ}\text{C}$	14	16	Hz	
$T_j$	Junction temperature for thermal shut-down		145		$^{\circ}\text{C}$	

Fig. 2 - AC test circuit



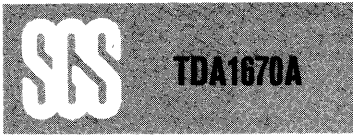
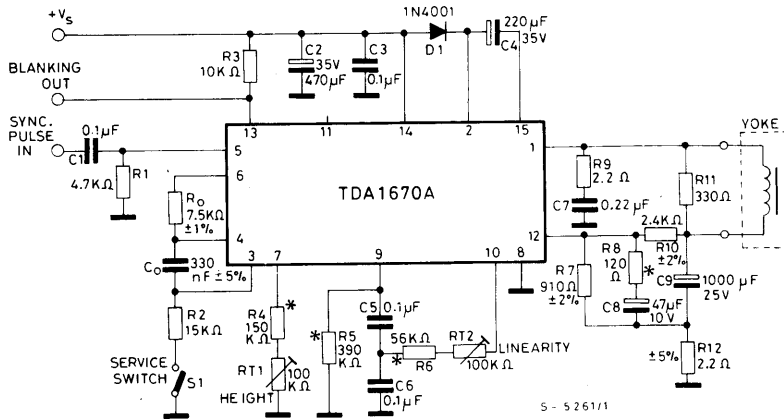


Fig. 3 - Application circuit for small screen 90° TVC set ( $R_y = 15\ \Omega$ ;  $L_y = 30\ \text{mH}$ ,  $I_y = 0.82\ \text{App}$ )



\* The value depends on the characteristics of the CRT. The value shown is indicative only.

### Typical performance

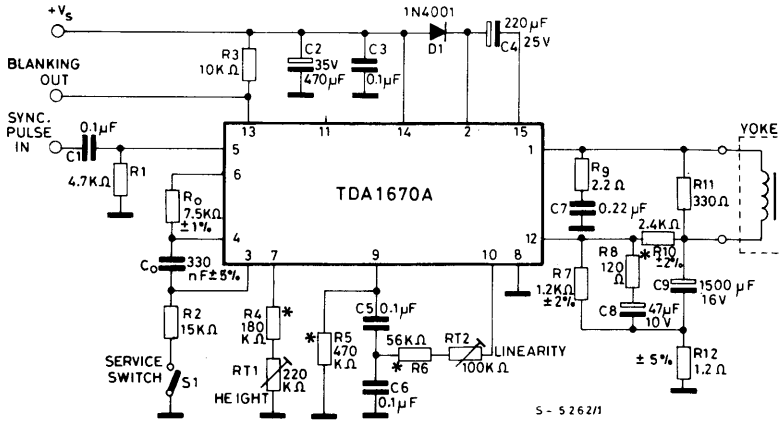
$V_s$	Minimum supply voltage	25	V
$I_s$	Supply current	140	mA
$t_{fly}$	Flyback time	0.7	msec
$t_{blkg}$	Blanking time	1.4	msec
$f_o$	Free running frequency	43.5	Hz
* $P_{tot}$	Power dissipation	2.4	W
* $R_{th}$ heatsink	Thermal resistance of the heatsink		
	for $T_{amb} = 60^\circ\text{C}$ and $T_j \text{ max} = 110^\circ\text{C}$	13	$^\circ\text{C/W}$
	for $T_{amb} = 60^\circ\text{C}$ and $T_j \text{ max} = 120^\circ\text{C}$	16	$^\circ\text{C/W}$

\* Worst case condition.



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Fig. 4 - Application circuit for 110° TVC set ( $R_y = 9.6\Omega$ ;  $L_y = 24.6 \text{ mH}$ ;  $I_y = 1.2 \text{ App}$ )



\* The value depends on the characteristics of the CRT. The value shown is indicative only.

### Typical performance

$V_s$	Minimum supply voltage	22.5	V
$I_s$	Supply current	185	mA
$t_{fly}$	Flyback time	1	msec
$t_{blkg}$	Blanking time	1.4	msec
$f_o$	Free running frequency	43.5	Hz
$P_{tot}$	Power dissipation	2.7	W
$R_{th}$ with heatsink	Thermal resistance for the heatsink		
	for $T_{amb} = 60^\circ\text{C}$ and $T_{j \text{ max}} = 110^\circ\text{C}$	11.5	$^\circ\text{C/W}$
	for $T_{amb} = 60^\circ\text{C}$ and $T_{j \text{ max}} = 120^\circ\text{C}$	14.5	$^\circ\text{C/W}$

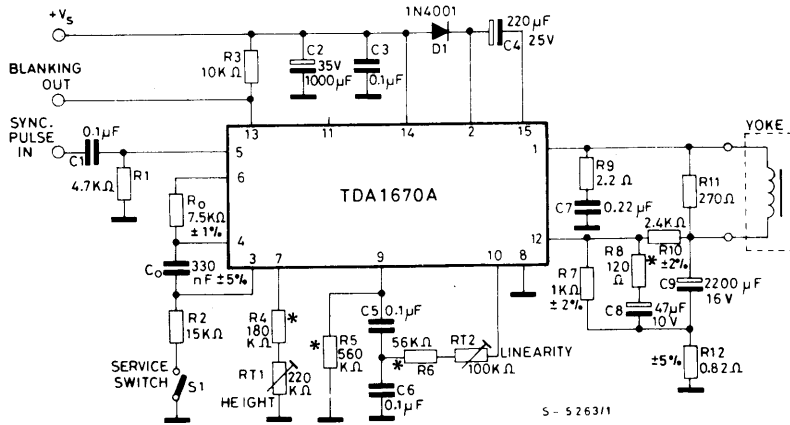
† Worst case condition.





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Fig. 5 - Application circuit for 110° TVC set ( $R_y = 5.9\Omega$ ;  $L_y = 10\text{ mH}$ ;  $I_y = 1.95\text{ App}$ )



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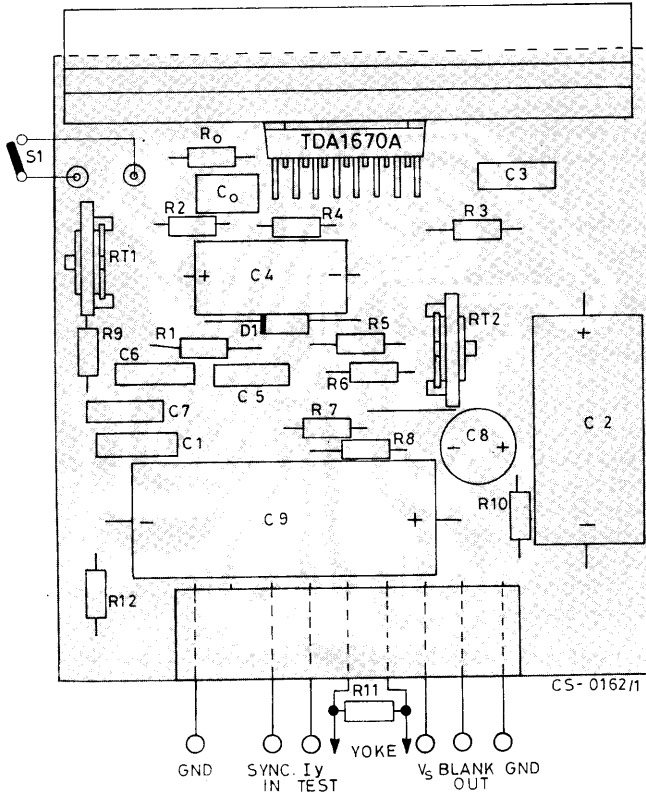
\* The value depends on the characteristics of the CRT. The value shown is indicative only.

## Typical performance

$V_s$	Minimum supply voltage	24	V
$I_s$	Supply current	285	mA
$t_{fly}$	Flyback time	0.6	msec
$t_{blkg}$	Blanking time	1.4	msec
$f_o$	Free running frequency	43.5	Hz
* $P_{tot}$	Power dissipation	4.3	W
* $R_{th\ heatink}$	Thermal resistance of the heatsink		
	for $T_{amb} = 60^\circ\text{C}$ and $T_j\text{ max} = 110^\circ\text{C}$	6.5	$^\circ\text{C}/^\circ\text{C}$
	for $T_{amb} = 60^\circ\text{C}$ and $T_j\text{ max} = 120^\circ\text{C}$	8.5	$^\circ\text{C}$

\* Worst case condition.

Fig. 6 - PC board and components layout for the application circuits of fig. 3, 4 and 5 (1 : 1 scale)



### APPLICATION INFORMATION (Refer to the block diagram)

#### Oscillator and Sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches  $R_o$  high or low so allowing the charge or the discharge of  $C_o$  under constant current conditions.

The Sync input pulse at the Sync gate lowers the level of the upper threshold and then it controls the period duration. A clock pulse is generated.

**Pin 4** is the inverting input of the amplifier used as integrator.

**Pin 6** is the output of the switch driven by the internal clock pulse generated by the threshold circuits.

**Pin 3** is the output of the amplifier.

**Pin 5** is the input for sync pulses (positive)



### Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.

The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor; a new voltage ramp is immediately allowed.

The required value of the capacitance is obtained by means of the series of two capacitors,  $C_a$  and  $C_b$ , which allow the linearity control by applying a feedback between the output of the buffer and the tapping from  $C_a$  and  $C_b$ .

- Pin 7** The resistance between pin 7 and ground defines the current mirror current and then the height of the scanning.
- Pin 9** is the output of the current mirror that charges the series of  $C_a$  and  $C_b$ . This pin is also the input of the buffer stage.
- Pin 10** is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through  $R_1$ .

### Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.

The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.

The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

- Pin 12** is the inverting input of the amplifier. An external network,  $R_a$  and  $R_b$ , defines the DC level across  $C_y$  so allowing a correct centering of the output voltage. The series network  $R_c$  and  $C_c$ , in conjunction with  $R_a$  and  $R_b$ , applies at the feedback input pin 12 a small part of the parabola, available across  $C_y$ , and the AC feedback voltage, taken across  $R_f$ . The external components  $R_c$ ,  $R_a$  and  $R_d$ , produce the linearity correction on the output scanning current  $I_y$  and their values must be optimized for each type of CRT.
- Pin 11** is the non-inverting input and it is not used. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.  
This pin is only used on a quasi-bridge configuration.
- Pin 1** is the output of the power amplifier and it drives the yoke by a negative slope current ramply.  $R_e$  and the Boucherot cell are used to stabilize the power amplifier.
- Pin 2** The supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage  $V_s$  by a diode, while during the retrace time this pin is supplied from the flyback generator.

### Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).

The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 14, the flyback pulse front end drives the flyback

generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.

An integrated diode stops the rising of this output increase and the voltage jump is transferred by means of capacitor Cf at the supply voltage  $V_{in}$  of the power stage (pin 2).

When the current across the yoke changes its direction, the output of the flyback generator falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.

Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 1) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

**Pin 15** is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 2 (see pin 2).

### Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

**Pin 13** is an open collector output where the blanking pulse is available.

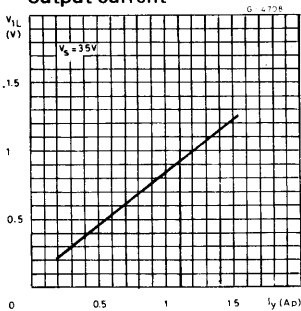
### Voltage regulator

The main supply voltage  $V_s$  is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

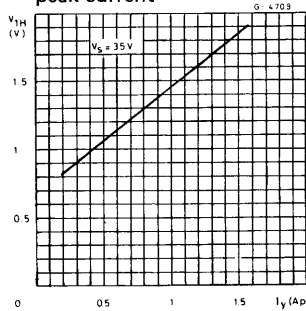
**Pin 14** is the main supply voltage input  $V_s$  (positive).

**Pin 8** is the GND pin or the negative input of  $V_s$ .

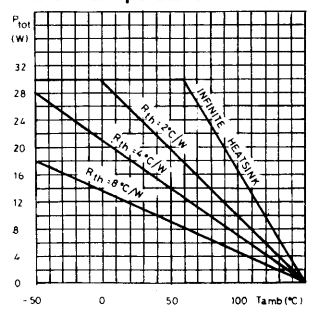
**Fig. 7 - Output saturation voltage to ground vs. peak output current**



**Fig. 8 - Output saturation voltage to supply vs. output peak current**



**Fig. 9 - Maximum allowable power dissipation vs. ambient temperature**





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## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink. Thanks to the MULTIWATT<sup>®</sup> package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 10 - Mounting example

