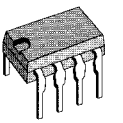
SGS-THOMSON MICROELECTRONICS

TSH151

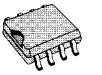
WIDE BANDWIDTH AND MOS INPUTS SINGLE OPERATIONAL AMPLIFIERS

PRELIMINARY DATA

- LOW DISTORTION
- GAIN BANDWIDTH PRODUCT : 150MHz
- UNITY GAIN STABLE
- SLEW RATE : 200V/µs
- VERY FAST SETTLING TIME : 70ns (0.1%)
- VERY HIGH INPUT IMPEDANCE



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION:

The TSH151 is a wideband monolithic operational amplifier, internally compensated for unity-gain stability.

The TSH151 features extremely high input impedance (typically greater than $10^{12}\Omega$) allowing direct interfacing with high impedance sources.

Low distortion, wide bandwidth and high linearity make this amplifier suitable for RF and video applications. Short circuit protection is provided by an internal current-limiting circuit.

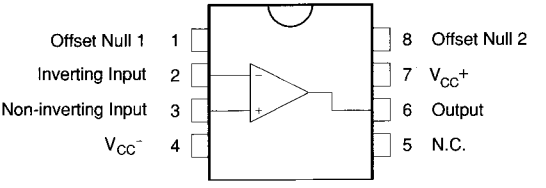
The THS151 has internal electrostatic discharge (ESD) protection circuits and fulfills MILSTD833C-Class2.

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
TSH151C	0°C, 70°C	•	•
TSH151I	-40°C, 105°C	•	•
TSH151M	-55°C, 125°C	•	•

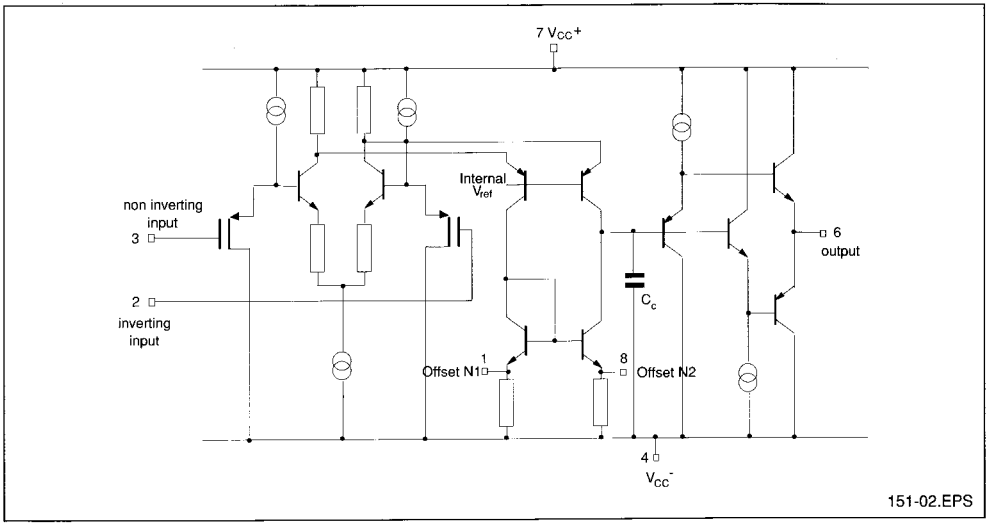
151-01.TBL

PIN CONNECTIONS (top view)

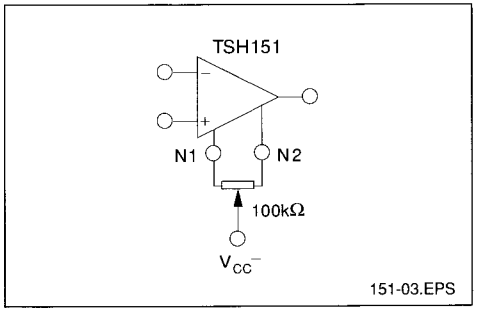


151-01.EPS

SCHEMATIC DIAGRAM



INPUT OFFSET VOLTAGE NULL CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±7	V
V_{id}	Differential Input Voltage		±5	V
V_i	Input Voltage Range		±5	V
I_{in}	Current On Offset Null Pins		±20	mA
T_{oper}	Operating Free-Air Temperature Range	TSH151C TSH151I TSH151M	0°C, 70°C -40°C, 105°C -55°C, 125°C	°C

151-02.TBL

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	±3 to ±6	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- to V_{CC}^+ -3	V

151-03.TBL

ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 5V$, $T_{amb} = 25°C$ (unless otherwise specified)

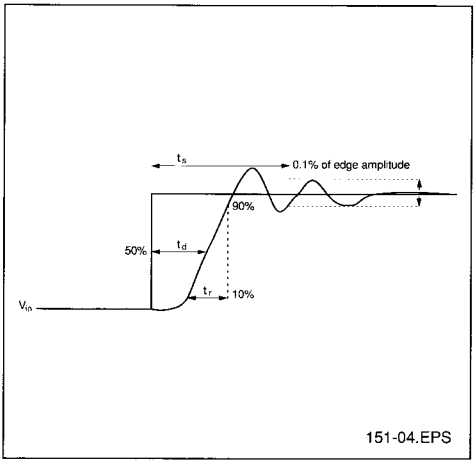
Symbol	Parameter		TSH151C, I, M			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage			0.15	10	mV
DV_{io}	Input Offset Voltage Drift $T_{min} \le T_{amb} \le T_{max}$			10		µV/°C
I_{ib}	Input Bias Current			25	300	pA
I_{io}	Input Offset Current			5	40	pA
I_{CC}	Supply Current, no load					mA
		$V_{CC} = \pm 5V$		23	30	
		$V_{CC} = \pm 3V$		21	28	
		$V_{CC} = \pm 6V$		25	40	
A_{vd}	Large Signal Voltage Gain $V_o = \pm 2.5V$					V/V
		$R_L = \infty$	800	1300		
		$R_L = 100\Omega$	300	850		
		$R_L = 50\Omega$	200	650		
V_{icm}	Input Common Mode Voltage Range		-5 to +2	-5.5 to +2.5		V
CMR	Common Mode Rejection Ratio	$V_{ic} = V_{icm\ min.}$	60	100		dB
SVR	Supply Voltage Rejection Ratio $V_{CC} = \pm 5V$ to $\pm 3V$		50	70		dB
V_o	Output Voltage	$R_L = 100\Omega$	± 3	+3.5 -3.7		V
		$R_L = 50\Omega$	± 2.8	+3.3 -3.5		
I_o	Output Short Circuit Current $V_{id} = \pm 1V$, $V_o = 0V$		±50	±100		mA
GBP	Gain Bandwidth Product $A_V = 100$, $R_L = 100\Omega$, $C_L = 15pF$, f = 7.5MHz			150		MHz
SR	Slew Rate $V_{in} = \pm 2V$, $A_v = 1$, $R_L = 100\Omega$, $C_L = 15pF$		100	200		V/µs
e_n	Equivalent Input Voltage Noise $R_S = 10\Omega$					$\frac{nV}{\sqrt{Hz}}$
		f = 1kHz		19.5		
		f = 10kHz		18		
		f = 100kHz		18		
		f = 1MHz		18		
	$R_S = 50\Omega$					
		fo = 1kHz		20		
		fo = 10kHz		18.2		
		fo = 100kHz		18.1		
		fo = 1MHz		18.2		
K_{ov}	Overshoot $V_{in} = \pm 2V$, $A_v = 1$, $R_L = 100\Omega$, $C_L = 15pF$			10		%
t_s	Settling Time 0.1% - (note 1) $V_{in} = \pm 1V$, $A_v = -1$			70		ns
t_r, t_f	Rise and Fall Time - (note 1) $V_{in} = \pm 100mV$, $A_V = 2$			5		ns
t_d	Delay Time - (note 1) $V_{in} = \pm 100mV$, $A_V = 2$			4		ns
Øm	Phase Margin $A_v = 2$, $R_L = 100\Omega$, $C_L = 15pF$			42		Degrees
THD	Total Harmonic Distortion $A_v = 10$, f = 1KHz, $V_o = \pm 2.5V$, no load			0.02		%
FPB	Full Power Bandwidth - (note 2) V_o = 5Vpp, $R_L = 100\Omega$			13		MHz
	V_o = 2Vpp, $R_L = 100\Omega$			32		

151-04.TBL

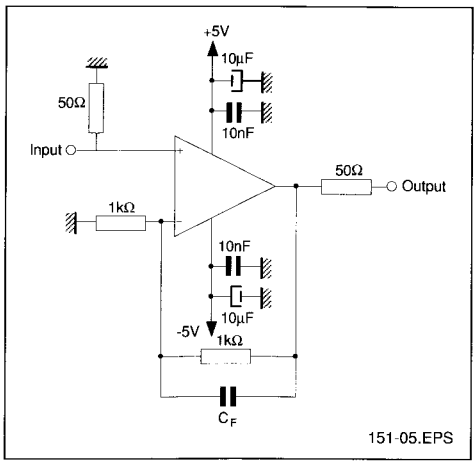
Note 1 : See test waveform figure

Note 2 : Full power bandwidth = $\frac{SR}{\Pi\ V_{opp}}$

TEST WAVEFORM



EVALUATION CIRCUIT



PRINTED CIRCUIT LAYOUT

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performance from your high speed op amp.

From the most to the least important points :

- Each power supply lead has to be bypassed to ground with a 1nF ceramic capacitor very close to the device and a 10uF tantalum capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op amp inputs. This is in order to decrease parasitic capacitor and inductance.
- Use small resistor values to decrease time constant with parasitic capacitor.
- Choose component sizes as small as possible (SMD).
- On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. One can also add a serial resistor in order to minimise its influence.
- One can add in parallel with feedback resistor a few pF ceramic capacitor C_F adjusted to optimize the settling time.