

$\mu\text{A}148 \bullet \mu\text{A}248 \bullet \mu\text{A}348$

Quad Operational Amplifiers

Linear Division Operational Amplifiers

Description

The $\mu\text{A}148$ series is a true quad $\mu\text{A}741$. It consists of four independent, high gain, internally frequency compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar $\mu\text{A}741$ operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single $\mu\text{A}741$ type operational amplifier.

Other features include input offset currents and input bias currents which are much less than those of a standard $\mu\text{A}741$. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

- $\mu\text{A}741$ Op Amp Operating Characteristics
- Low Supply Current Drain
- Class AB Output Stage — No Crossover Distortion
- Lead Compatible With The $\mu\text{A}324$ & $\mu\text{A}3403$
- Low Input Offset Voltage — 1.0 mV Typically
- Low Input Offset Current — 4.0 nA Typically
- Low Input Bias Current — 30 nA Typically
- Gain Bandwidth Product For $\mu\text{A}148$ (Unity Gain) — 1.0 MHz Typically
- High Degree Of Isolation Between Amplifiers — 120 dB Typically
- Overload Protection For Inputs And Outputs

Absolute Maximum Ratings

Storage Temperature Range

Ceramic DIP	-65°C to +175°C
Molded DIP	-65°C to +150°C

Operating Temperature Range

Extended ($\mu\text{A}148\text{M}$)	-55°C to +125°C
Industrial ($\mu\text{A}248\text{V}$)	-25°C to +85°C
Commercial ($\mu\text{A}348\text{C}$)	0°C to +70°C

Lead Temperature

Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C

Internal Power Dissipation^{1,2}

14L-Molded DIP	1.04 W
14L-Ceramic DIP	1.36 W

Supply Voltage

$\mu\text{A}148$	± 22 V
$\mu\text{A}248$, $\mu\text{A}348$	± 18 V

Differential Input Voltage

$\mu\text{A}148$	± 44 V
$\mu\text{A}248$, $\mu\text{A}348$	± 36 V

Input Voltage

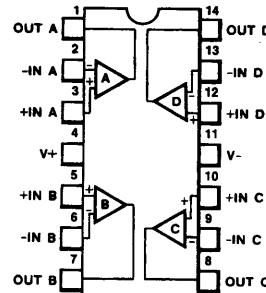
$\mu\text{A}148$	± 22 V
$\mu\text{A}248$, $\mu\text{A}348$	± 18 V

Output Short Circuit Duration³

Indefinite

Connection Diagram

14-Lead DIP
(Top View)



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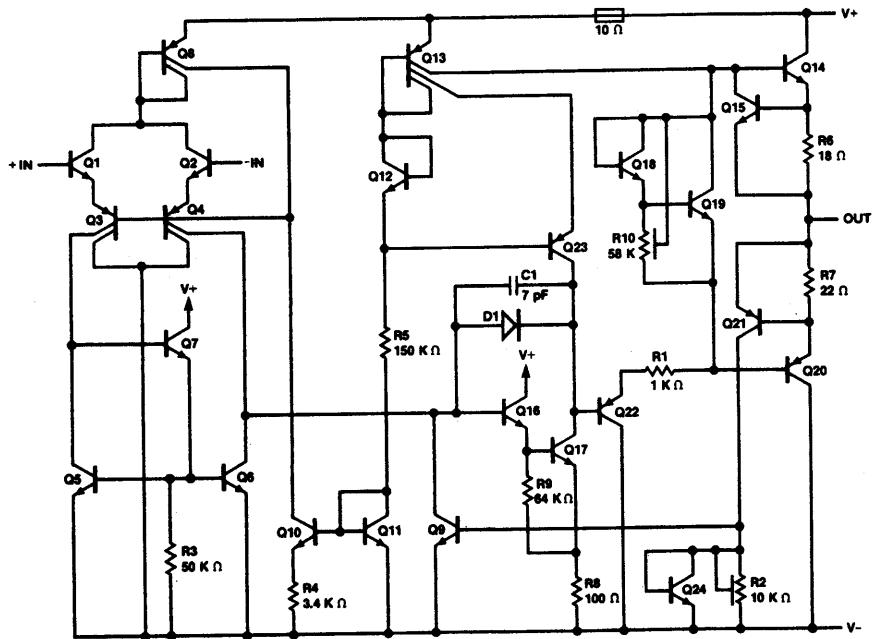
Order Information

Device Code	Package Code	Package Description
$\mu\text{A}148\text{DM}$	6A	Ceramic DIP
$\mu\text{A}248\text{DV}$	6A	Ceramic DIP
$\mu\text{A}248\text{PV}$	9A	Molded DIP
$\mu\text{A}348\text{DC}$	6A	Ceramic DIP
$\mu\text{A}348\text{PC}$	9A	Molded DIP

Notes

1. $T_{J\ Max} = 150^\circ\text{C}$ for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C . Above this temperature, derate the 14-Lead Molded DIP at $8.3 \text{ mW}/^\circ\text{C}$, and the 14-Lead Ceramic DIP at $9.1 \text{ mW}/^\circ\text{C}$.
3. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Equivalent Circuit (1/4 of Circuit)



□ = CROSSUNDER

EO00001F

μ A148

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$		1.0	5.0	mV
I_{IO}	Input Offset Current			4	25	nA
I_{IB}	Input Bias Current			30	100	nA
Z_I	Input Impedance		0.8	2.5		M Ω
I_{CC}	Supply Current (Total)			2.4	3.6	mA
I_{OS}	Output Short Circuit Current			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0 \text{ k}\Omega$	50	160		V/mV
CS	Channel Separation	1.0 Hz $\leq f \leq 20$ kHz (Input Referred)		-120		dB

The following specifications apply over the range of $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$.

V_{IO}	Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$			6.0	mV
I_{IO}	Input Offset Current				75	nA
I_{IB}	Input Bias Current				325	nA
CMR	Common Mode Rejection	$R_S \leq 10 \text{ k}\Omega$	70	90		dB
V_{IR}	Input Voltage Range		± 12			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$	77	96		dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0 \text{ k}\Omega$	25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10 \text{ k}\Omega$	± 12	± 13		V
		$R_L = 2.0 \text{ k}\Omega$	± 10	± 12		

AC Characteristics

BW	Bandwidth			1.0		MHz
ϕ	Phase Margin	$A_V = 1.0$		60		degrees
SR	Slew Rate	$A_V = 1.0$		0.5		V/ μ s

μ A248

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			4	50	nA
I_{IB}	Input Bias Current			30	200	nA
Z_I	Input Impedance		0.8	2.5		M Ω
I_{CC}	Supply Current (Total)			2.4	4.5	mA
I_{OS}	Output Short Circuit Current			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0 \text{ k}\Omega$	25	160		V/mV
CS	Channel Separation	1.0 Hz $\leq f \leq 20$ kHz (Input Referred)		-120		dB

The following specifications apply over the range of $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$.

V_{IO}	Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$			7.5	mV
I_{IO}	Input Offset Current				125	nA
I_{IB}	Input Bias Current				500	nA
CMR	Common Mode Rejection	$R_S \leq 10 \text{ k}\Omega$	70	90		dB
V_{IR}	Input Voltage Range		± 12			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$	77	96		dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0 \text{ k}\Omega$	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10 \text{ k}\Omega$	± 12	± 13		V
		$R_L = 2.0 \text{ k}\Omega$	± 10	± 12		

AC Characteristics

BW	Bandwidth			1.0		MHz
ϕ	Phase Margin	$A_V = 1.0$		60		degrees
SR	Slew Rate	$A_V = 1.0$		0.5		V/ μ s

μ A348

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15$ V, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$		1.0	6.0	mV
I_{IO}	Input Offset Current			4	50	nA
I_{IB}	Input Bias Current			30	200	nA
Z_I	Input Impedance		0.8	2.5		M Ω
I_{CC}	Supply Current (Total)			2.4	4.5	mA
I_{OS}	Output Short Circuit Current			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0 \text{ k}\Omega$	25	160		V/mV
CS	Channel Separation	1.0 Hz $\leq f \leq 20$ kHz (Input Referred)		-120		dB

The following specifications apply over the range of $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

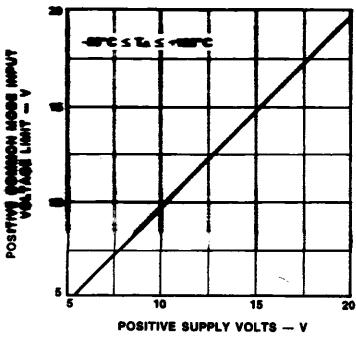
V_{IO}	Input Offset Voltage	$R_S \leq 10 \text{ k}\Omega$			7.5	mV
I_{IO}	Input Offset Current				100	nA
I_{IB}	Input Bias Current				400	nA
CMR	Common Mode Rejection	$R_S \leq 10 \text{ k}\Omega$	70	90		dB
V_{IR}	Input Voltage Range		± 12			V
PSRR	Power Supply Rejection Ratio	$R_S \leq 10 \text{ k}\Omega$	77	96		dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L \geq 2.0 \text{ k}\Omega$	15			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10 \text{ k}\Omega$	± 12	± 13		V
		$R_L = 2.0 \text{ k}\Omega$	± 10	± 12		

AC Characteristics

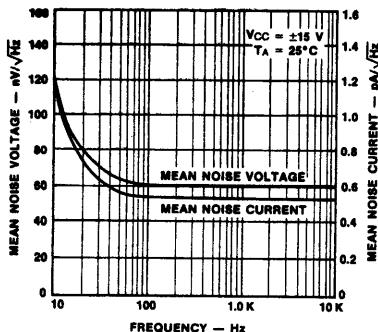
BW	Bandwidth			1.0		MHz
ϕ	Phase Margin	$A_V = 1.0$		60		degrees
SR	Slew Rate	$A_V = 1.0$		0.5		V/ μ s

Typical Performance Curves

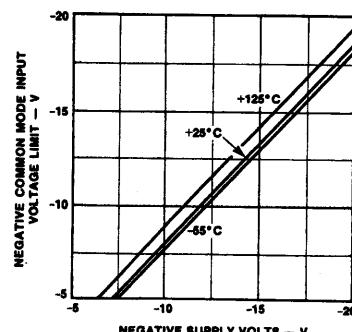
Positive Common Mode Input Voltage Limit vs Supply Voltage



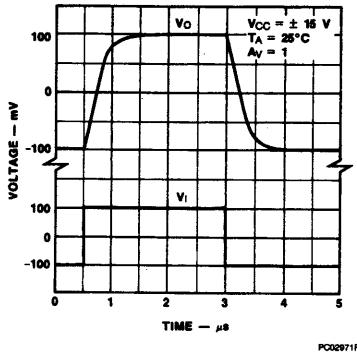
Input Noise Voltage and Noise Current vs Frequency



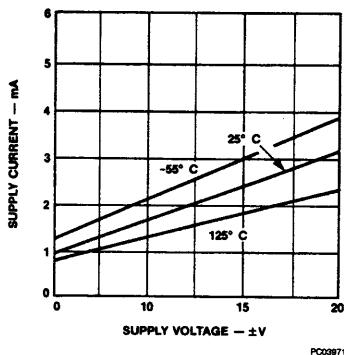
Negative Common Mode Input Voltage Limit vs Supply Voltage



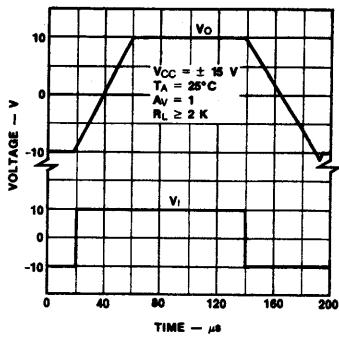
Small Signal Pulse Response



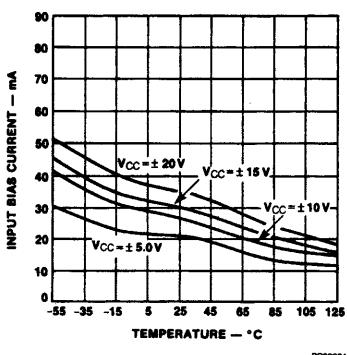
Supply Current vs Power Supply Voltage



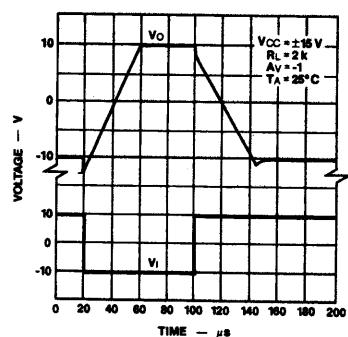
Large Signal Pulse Response



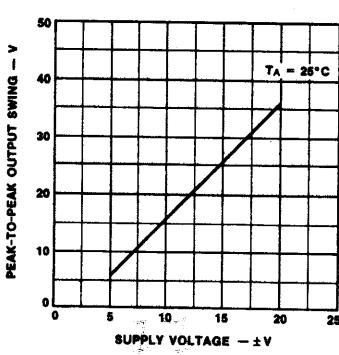
Input Bias Current vs Ambient Temperature



Inverting Large Signal Pulse Response

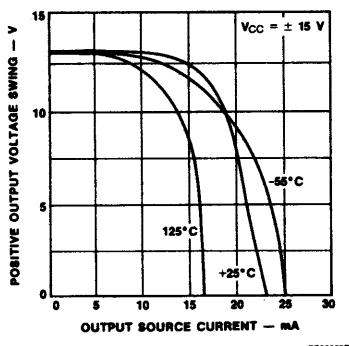


Output Voltage Swing vs Supply Voltage

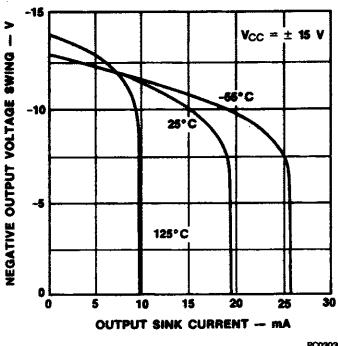


Typical Performance Curves (Cont.)

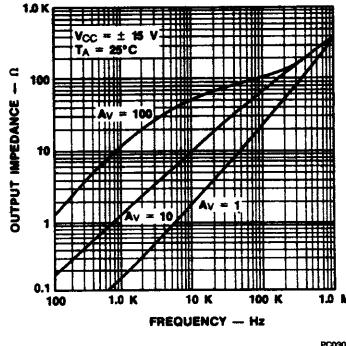
Output Voltage vs
Source Current



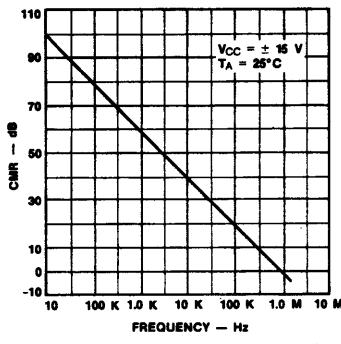
Output Voltage vs
Sink Current



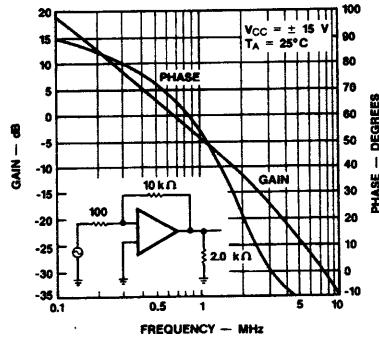
Output Impedance vs
Frequency



CMR vs Frequency



Gain and Phase vs Frequency



Gain Bandwidth vs
Temperature

