FAIRCHILD
A Schlumberger Company

μA9645(3245) Quad TTL To MOS/CCD Driver

Linear Division Interface Products

Description

The μA9645(3245) is a high speed driver intended to be used as a clock (high level) driver for 18 or 22-lead dynamic NMOS RAMs. It also satisfies the non-overlapping phase clock drive requirements for CCD memories like the F464 (64K) RAM.

The circuit is designed to operate on nominal +5.0 V and +12 V power supplies and contains input and output clamp diodes to minimize line reflections.

The device features two common enable inputs, a refresh select input and a clock control input. Internal gating structure is organized so that all four drivers may be deactivated for standby operation, or a single driver may be deactivated for read/write operation or all four drivers may be activated for refresh operation.

The μA9645(3245) is a lead for lead replacement of the Intel 3245 Quad TTL-to-MOS Driver, with substantially reduced DC power dissipation.

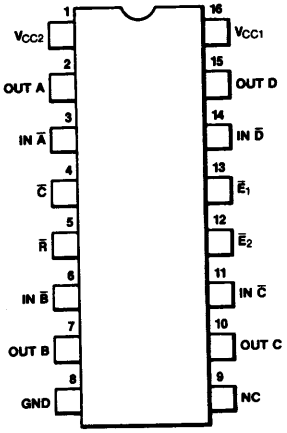
- **Interchangeable With Intel 3245**
- **Four High Speed, High Current Drivers**
- **Control Logic Optimized For MOS RAMs**
- **Satisfies CCD Memory And Delay Line Drive Requirements**
- **TTL And DTL Compatible Inputs**
- **High Voltage Schottky Technology**

Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Thermal Power Dissipation[1,2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage, V_{CC1}	−0.5 V to +7.0 V
Supply Voltage, V_{CC2}	−0.5 V to +14.0 V
All Input Voltages	−1.0 V to V−
Outputs For Clock Driver	−1.0 V to (V−) +1.0 V
Temperature Under Bias	−10°C to +70°C

Notes
1. $T_{J\ Max}$ = 175°C for the Ceramic DIP, and 150°C for the Molded DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram 16-Lead DIP (Top View)



Order Information

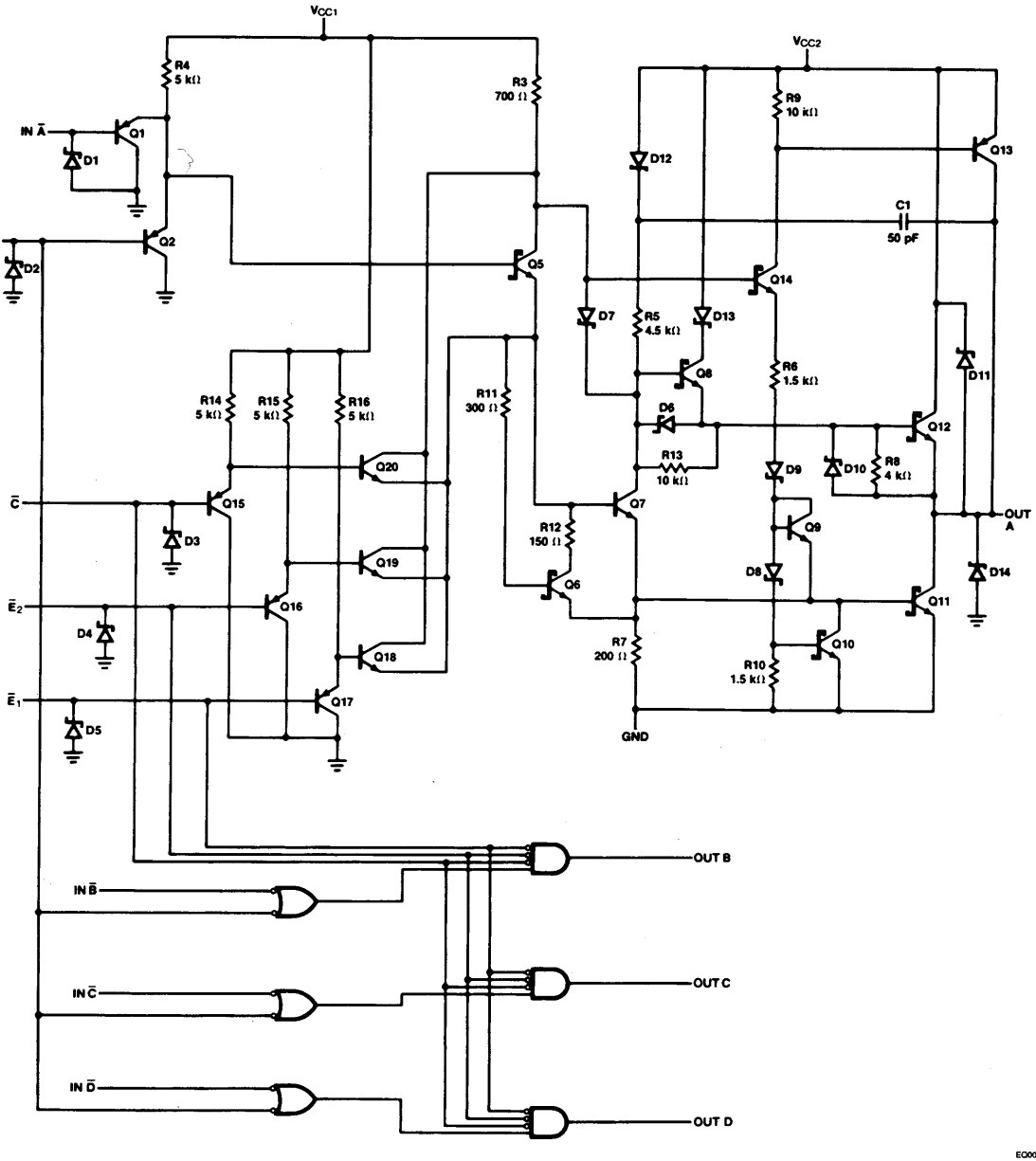
Device Code	Package Code	Package Description
μA9645DC(3245)	7B	Ceramic DIP
μA9645PC(3245)	9B	Molded DIP

Truth Table

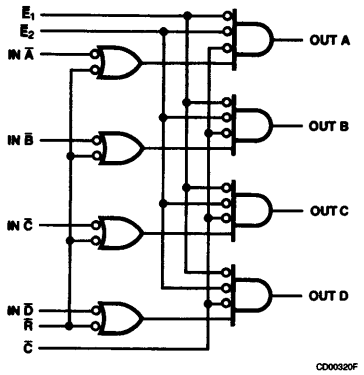
Inputs					Output
Control			Address		
$\overline{C}$	$\overline{E}_2$	$\overline{E}_1$	INPUT	REFRESH	
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	H	L
L	L	L	L	X	H
L	L	L	X	L	H

H = HIGH
L = LOW
X = Don't Care

Equivalent Circuit



gic Diagram



645(3245)

ctrical Characteristics V_{CC1} = 5.0 V ±5%, V_{CC2} = 12 V ±5%, T_A = 0°C to 70°C, unless otherwise specified.

C Characteristics

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{ID}	Input Load Current, IN ($\overline{A}$,$\overline{B}$,$\overline{C}$,$\overline{D}$)	V_F = 0.45 V			−0.25	mA
I_{IE}	Input Load Current, $\overline{R}$, $\overline{C}$, $\overline{E}_1$, $\overline{E}_2$	V_F = 0.45 V			−1.0	mA
I_{ID}	Data Input Leakage Current	V_R = 5.0 V			10	μA
I_{IE}	Enable Input Leakage Current	V_R = 5.0 V			40	μA
V_{OL}	Output Voltage LOW	I_{OL} = 5.0 mA, V_{IH} = 2.0 V			0.45	V
		I_{OL} = −5.0 mA	−1.0			
V_{OH}	Output Voltage HIGH	I_{OH} = −1.0 mA, V_{IL} = 0.8 V	V_{CC2}−0.50			V
		I_{OH} = 5.0 mA			V_{CC2} + 1.0	
V_{IL}	Input Voltage LOW, All Inputs				0.8	V
V_{IH}	Input Voltage HIGH, All Inputs		2.0			V
I_{CCH}	Positive Supply Current HIGH	V_{CC1} = 5.25 V		13	20	mA
I_{EEH}	Negative Supply Current HIGH	V_{CC2} = 12.6 V		14	20	mA
$P_{D(H)}$	Power Consumption HIGH	All Outputs HIGH		248	357	mW
	Power Per Channel			62	90	mW
I_{CCL}	Positive Supply Current LOW	V_{CC1} = 5.25 V		27	35	mA
I_{EEL}	Negative Supply Current LOW	V_{CC2} = 12.6 V		12	15	mA
$P_{D(L)}$	Power Consumption LOW	All Outputs LOW		296	373	mW
	Power Per Channel			74	94	mW

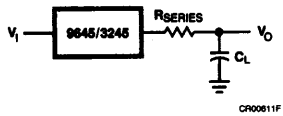
μA9645(3245) (Cont.)
Electrical Characteristics $V_{CC1} = 5.0\ V \pm 5\%$, $V_{CC2} = 12\ V \pm 5\%$, $T_A = 0°C$ to $70°C$, unless otherwise specified.

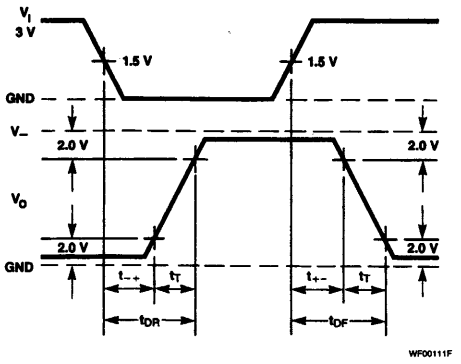
AC Characteristics

Symbol	Characteristic	Condition	Min[1]	Typ[2,4]	Max[3]	Unit
t−(+)	Input to Output Delay	$R_{SERIES} = 0$	5.0	11		ns
t_{DR1}	Delay Plus Rise Time	$R_{SERIES} = 0$		18	32	ns
t+(−)	Input to Output Delay	$R_{SERIES} = 0$	3.0	7.0		ns
t_{DF1}	Delay Plus Fall Time	$R_{SERIES} = 0$		18	32	ns
t_T	Output Transition Time	$R_{SERIES} = 20\ \Omega$	10	13	20	ns
t_{DR2}	Delay Plus Rise Time	$R_{SERIES} = 20\ \Omega$		27	38	ns
t_{DF2}	Delay Plus Fall Time	$R_{SERIES} = 20\ \Omega$		24	38	ns

Notes
1. $C_L = 150$ pF
2. $C_L = 200$ pF
3. $C_L = 250$ pF
4. Typical values are measured at $T_A = 25°C$

AC Test Circuit and Waveforms





Note
AC Test Conditions:
Input Pulse Amplitude = 3.0 V
Input Pulse Rise and Fall Times = 5.0 ns Between 1.0 V and 2.0 V