FAIRCHILD
A Schlumberger Company

# μA685
# High Speed Single Latched Comparator

Linear Division Comparators

## Description

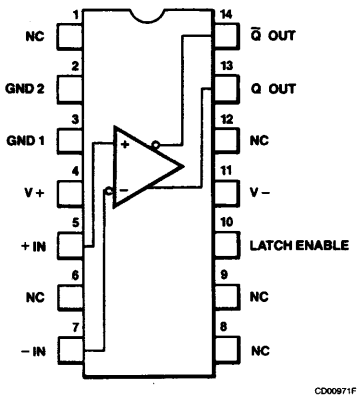
The μA685 is a fast voltage comparator manufactured with an advanced high speed bipolar process that makes possible very short propagation delays without sacrificing the excellent matching characteristics formerly associated only with slow, high performance linear ICs. The circuit has differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capability is adequate for driving terminated 50 Ω transmission lines. The low input offset and high resolution make this comparator especially suitable for high speed precision analog to digital processing.

A latch function is provided to allow the comparator to be used in a sample and hold mode. If the latch enable is HIGH, the comparator functions normally. When the latch enable is driven LOW, the comparator outputs are locked in their existing logical states. If the latch function is not used, the latch enable must be connected to ground.

The μA685 is lead compatible with the AM685.

- **6.5 ns Maximum Propagation Delay At 5.0 mV Overdrive**
- **3.0 ns Latch Set up Time**
- **Complementary ECL Outputs**
- **50 Ω Line Driving Capability**
- **Typical Output Skew 0.2 ns**
- **Constant Propagation Delay With Overdrive**

## Connection Diagram
## SO-14 Package
## (Top View)

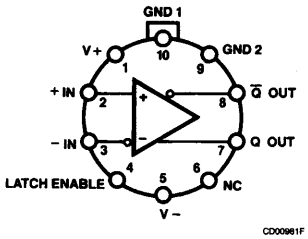



CD00971F

## Order Information

| Device Code | Package Code | Package Description |
|---|---|---|
| μA685SV | KD | Molded Surface Mount |

## Connection Diagram
## 10-Lead Metal Package
## (Top View)

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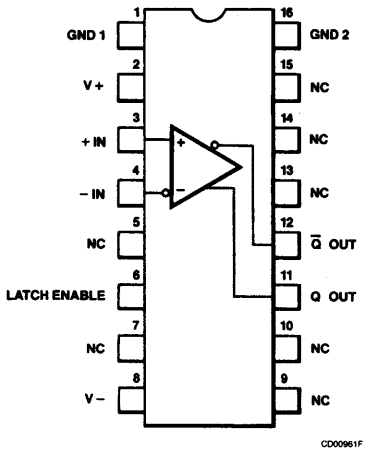
## Order Information

| Device Code | Package Code | Package Description |
|---|---|---|
| μA685HM | 5X | Metal |
| μA685HV | 5X | Metal |

## Connection Diagram
## 16-Lead DIP
## (Top View)

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## Order Information

| Device Code | Package Code | Package Description |
|---|---|---|
| μA685DM | 6B | Ceramic DIP |
| μA685DV | 6B | Ceramic DIP |
| μA685PV | 9B | Molded DIP |

## Absolute Maximum Ratings

| | |
|---|---|
| Storage Temperature Range | |
| Metal Can and Ceramic DIP | −65°C to +175°C |
| Molded DIP and SO-14 | −65°C to +150°C |
| Operating Temperature Range | |
| Extended (μA685M) | −55°C to +125°C |
| Industrial (μA685V) | −30°C to +85°C |
| Lead Temperature | |
| Metal Can and Ceramic DIP (soldering, 60 s) | 300°C |
| Molded DIP and SO-14 (soldering, 10 s) | 265°C |

| | |
|---|---|
| Internal Power Dissipation[1, 2] | |
| 10L-Metal Can | 1.07 W |
| 16L-Ceramic DIP | 1.50 W |
| 16L-Molded DIP | 1.04 W |
| SO-14 | 0.93 W |
| Positive Supply Voltage | +7.0 V |
| Negative Supply Voltage | −7.0 V |
| Input Voltage | ±4.0 V |
| Differential Input Voltage | ±6.0 V |
| Output Current | 30 mA |
| Minimum Operating Voltage (V+ to V−) | 9.7 V |

**Notes**

1. $T_{J\ Max}$ = 150°C for the Molded DIP and SO-14, and 175°C for the Metal Can and Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 10L-Metal Can at 7.1 mW/°C, the 16L-Ceramic DIP at 10 mW/°C, the 16L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.

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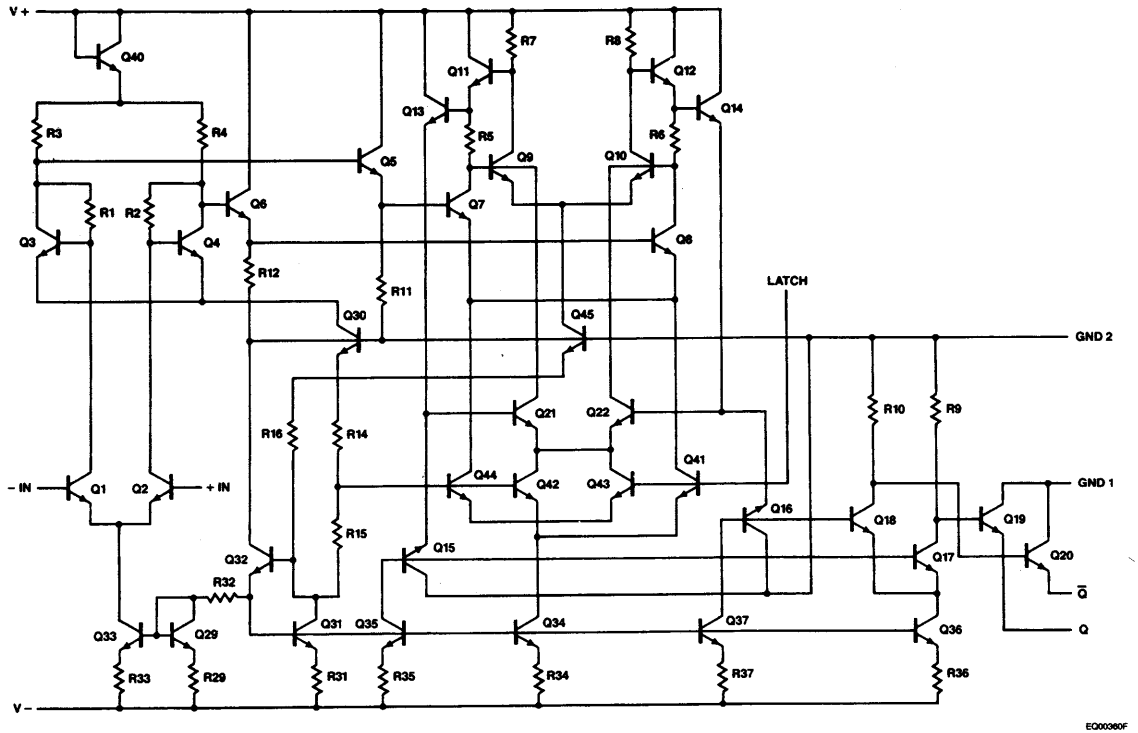
## Equivalent Circuit



## μA685

**Electrical Characteristics** Over recommended operating temperature and supply voltage ranges, unless otherwise specified.

**DC Characteristics**

| Symbol | Characteristic | Condition[2] | μA685V | | μA685M | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $V_{IO}$ | Input Offset Voltage | $R_S \leq 100\ \Omega$, $T_A = 25°C$ | −2.0 | +2.0 | −2.0 | +2.0 | mV |
| | | $R_S \leq 100\ \Omega$ | −2.5 | +2.5 | −3.0 | +3.0 | |
| $\Delta V_{IO}/\Delta T$ | Average Temperature Coefficient of Input Offset Voltage[3] | $R_S \leq 100\ \Omega$ | −10 | +10 | −10 | +10 | μV/°C |
| $I_{IO}$ | Input Offset Current[3] | $25°C \leq T_A \leq T_{A\ Max}$ | −1.0 | +1.0 | −1.0 | +1.0 | μA |
| | | $T_A = T_{A\ Min}$ | −1.3 | +1.3 | −1.6 | +1.6 | |
| $I_{IB}$ | Input Bias Current | $25°C \leq T_A \leq T_{A\ Max}$ | | 10 | | 10 | μA |
| | | $T_A = T_{A\ Min}$ | | 13 | | 16 | |
| $R_I$ | Input Resistance | $T_A = 25°C$ | 6.0 | | 6.0 | | kΩ |
| $C_I$ | Input Capacitance[1] | $T_A = 25°C$ | | 3.0 | | 3.0 | pF |
| $V_{CM}$ | Common Mode Voltage Range | | −3.3 | +3.3 | −3.3 | +3.3 | V |
| CMR | Common Mode Rejection | $R_S \leq 100\ \Omega$, $-3.3 \leq V_{CM} \leq +3.3V$ | 80 | | 80 | | dB |
| PSRR | Power Supply Rejection Ratio[3] | $R_S \leq 100\ \Omega$, $\Delta V_S = \pm 5\%$ | 70 | | 70 | | dB |
| $V_{OH}$ | Output Voltage HIGH | $T_A = 25°C$ | −0.960 | −0.810 | −0.960 | −0.810 | V |
| | | $T_A = T_{A\ Min}$ | −1.060 | −0.890 | −1.100 | −0.920 | |
| | | $T_A = T_{A\ Max}$ | −0.890 | −0.700 | −0.850 | −0.620 | |
| $V_{OL}$ | Output Voltage LOW | $T_A = 25°C$ | −1.850 | −1.650 | −1.850 | −1.650 | V |
| | | $T_A = T_{A\ Min}$ | −1.890 | −1.675 | −1.910 | −1.690 | |
| | | $T_A = T_{A\ Max}$ | −1.825 | −1.625 | −1.810 | −1.575 | |
| I+ | Positive Supply Current | | | 22 | | 22 | mA |
| I− | Negative Supply Current | | | 26 | | 26 | mA |
| $P_c$ | Power Consumption[4] | | | 300 | | 300 | mW |

**Switching Characteristics** $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV

| Symbol | Characteristic | Condition[2] | μA685V | | μA685M | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{PD+}$ | Input to Output HIGH[3] | $T_{A\ Min} \leq T_A \leq 25°C$ | | 6.5 | | 6.5 | ns |
| | | $T_A = T_{A\ Max}$ | | 9.5 | | 12 | |
| $t_{PD-}$ | Input to Output LOW[3] | $T_{A\ Min} \leq T_A \leq 25°C$ | | 6.5 | | 6.5 | ns |
| | | $T_A = T_{A\ Max}$ | | 9.5 | | 12 | |

## μA685 (Cont.)
## Electrical Characteristics

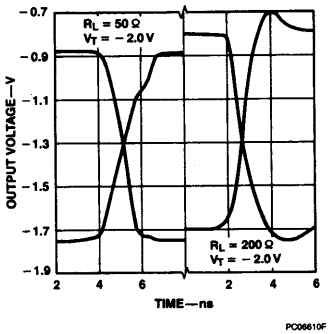
**Switching Characteristics** $V_{in}$ = 100 mV, $V_{OD}$ = 5.0 mV

| Symbol | Characteristic | Condition[2] | μA685V | | μA685M | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $t_{PD+}$ (E) | Latch Enable to Output HIGH Delay[3] | $T_{A\ Min} \leq T_A \leq 25°C$ | | 6.5 | | 6.5 | ns |
| | | $T_A = T_{A\ Max}$ | | 9.5 | | 12 | |
| $t_{PD-}$ (E) | Latch Enable to Output LOW Delay[3] | $T_{A\ Min} \leq T_A \leq 25°C$ | | 6.5 | | 6.5 | ns |
| | | $T_A = T_{A\ Max}$ | | 9.5 | | 12 | |
| $t_S$ | Minimum Set up Time[3] | $T_{A\ Min} \leq T_A \leq 25°C$ | | 3.0 | | 3.0 | ns |
| | | $T_A = T_{A\ Max}$ | | 4.0 | | 6.0 | |
| $t_h$ | Minimum Hold Time[3] | $T_{A\ Min} \leq T_A \leq T_{A\ Max}$ | | 1.0 | | 1.0 | ns |
| $t_{pw}$(E) | Minimum Latch Enable Pulse Width[3] | $T_{A\ Min} \leq T_A \leq 25°C$ | | 3.0 | | 3.0 | ns |
| | | $T_A = T_{A\ Max}$ | | 4.0 | | 5.0 | |

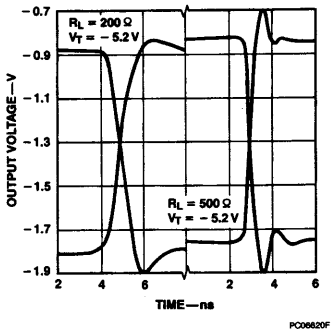
**Notes**
1. For TO-99 only; CERDIP = 7.0 pF.
2. Unless otherwise specified V+ = 6.0 V, V- = −5.2 V, $V_T$ = −2.0 V, and $R_L$ = 50 Ω; all switching characteristics are for a 100 mV input step with 5.0 mV overdrive. The specifications given for $V_{IO}$, $I_{IO}$, $I_{IB}$, CMR, PSRR, $t_{PD+}$ and $t_{PD-}$ apply over the full $V_{CM}$ range and for ±5% supply voltages. The μA685 is designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
3. Guaranteed, but not tested in production.
4. Refer to Internal Power Dissipation in Absolute Maximum Rating Table.

**Typical Performance Curves** $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV, unless otherwise specified.

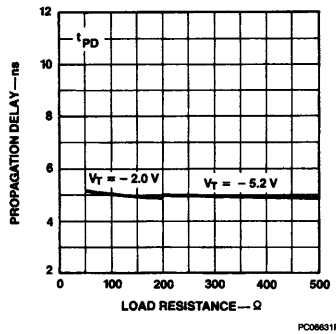
**Response for Various Load Resistances**



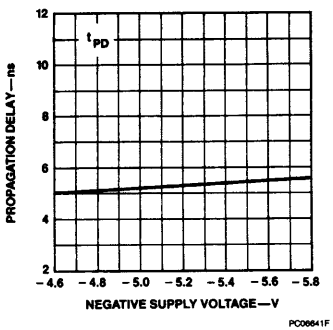

**Response for Various Load Resistances**



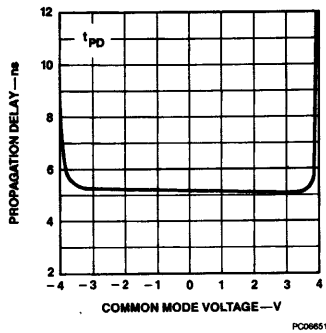

**Propagation Delay vs Load Resistance**



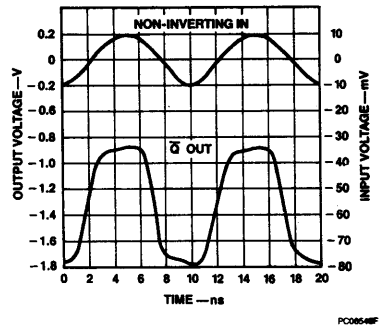

**Propagation Delay vs Negative Supply Voltage**



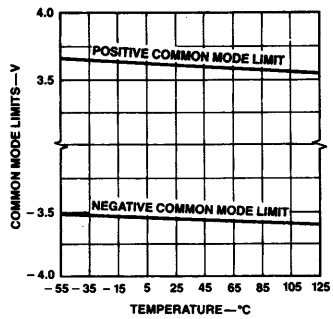

**Propagation Delay vs Common Mode Voltage**



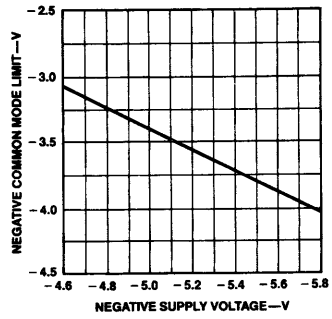

**Response to 100 MHz Sine Wave**



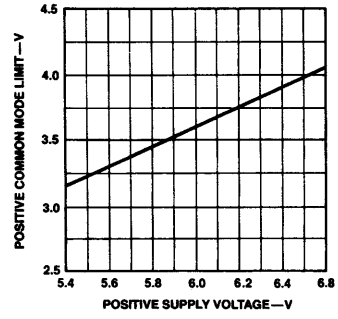

**Common Mode Limits vs Temperature**




**Negative Common Mode Limit vs Negative Supply Voltage**

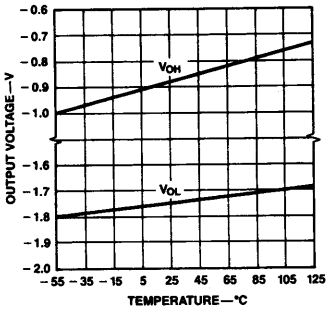



**Positive Common Mode Limit vs Positive Supply Voltage**



**Typical Performance Curves** (Cont.) $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV, unless otherwise specified.

### Output Levels vs Temperature



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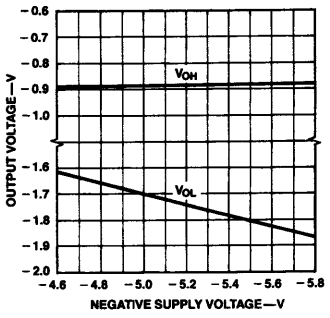
### Output Levels vs Negative Supply Voltage



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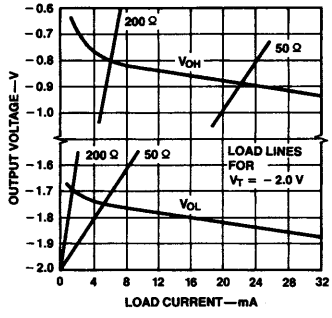
### Output Levels vs DC Loading



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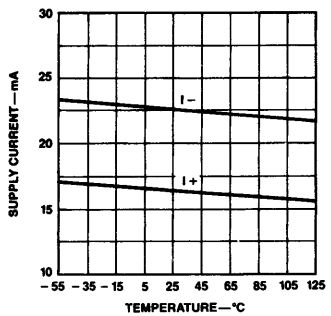
### Supply Currents vs Temperature



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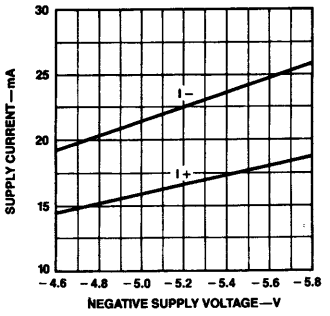
### Supply Currents vs Negative Supply Voltage



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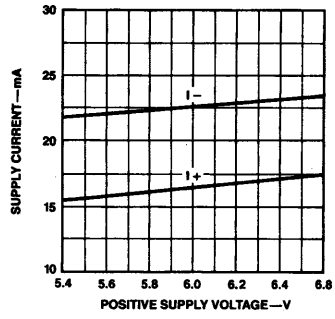
### Supply Currents vs Positive Supply Voltage



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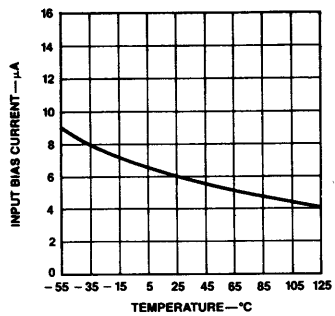
### Input Bias Current vs Temperature



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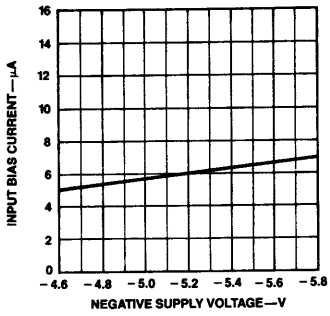
### Input Bias Current vs Negative Supply Voltage



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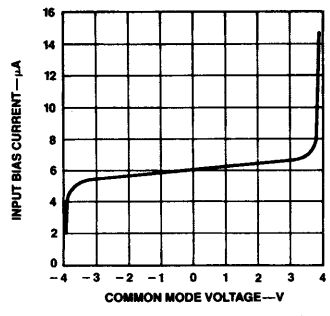
### Input Bias Current vs Common Mode Voltage



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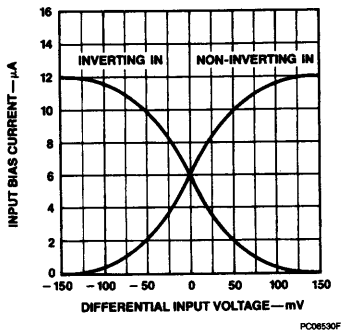
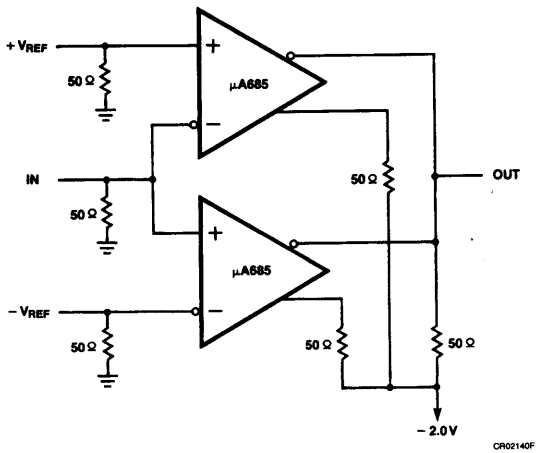
**Typical Performance Curves** (Cont.) $T_A = 25°C$, $V+ = 6.0$ V, $V- = -5.2$ V, $V_T = -2.0$ V, $R_L = 50\ \Omega$, and switching characteristics are for $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV, unless otherwise specified.

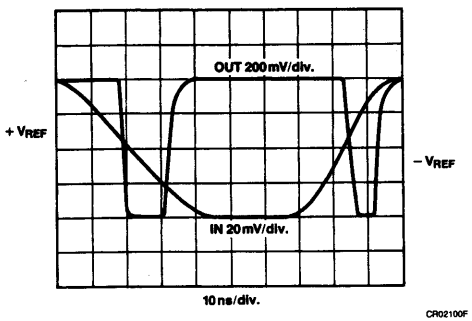
**Input Current vs Differential Input Voltage**




**Typical Applications** ($T_A = 25°C$)

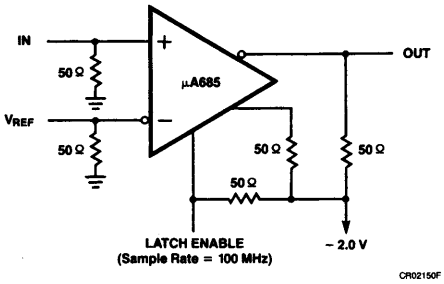
**High Speed Window Detector**

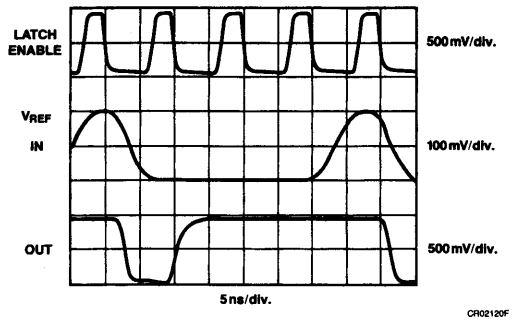


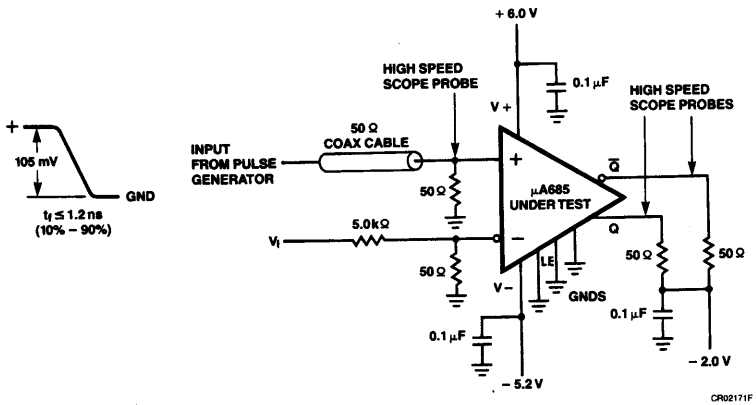
## Typical Applications (Cont.)

### High Speed Sampling




### Measurement Of Propagation Delay




Propagation delays $t_{PD}+$ ($\overline{Q}$ output) and $t_{PD}-$ (Q output) are measured with input signal conditions of a 100 mV step with an overdrive of 5.0 mV (the overdrive is the voltage in excess of that needed to bring the output to the center of its dynamic range). Offset is compensated for by adjusting $V_I$ until outputs are in the linear region while the Pulse Generator is disconnected. $V_I$ is then increased in the positive direction so inverting input changes by 5.0 mV, i.e. the overdrive condition. Propagation delays are then measured with actual input pulse condition of +105 mV to 0 V swing, with a $t_{PD}+$ or $t_{PD}-$ reading taken between the +5.0 mV level of the input pulse and the 50% point of the outputs.

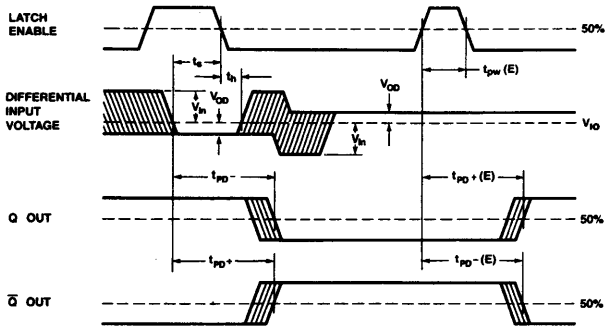
### Thermal Considerations

To achieve the high speed of the μA685, a certain amount of power must be dissipated as heat. This increases the temperature of the die relative to the ambient temperature. In order to be compatible with ECL III and ECL 10,000, which normally use air flow as a means of package cooling, the μA685 characteristics are specified when the device has an air flow across the package of 500 linear feet per minute or greater. Thus, even though different ECL circuits on a printed circuit board may have different power dissipations, all will have the same input and output levels, etc. provided each sees the same air flow and air temperature. This eases design, since the only change in characteristics between devices is due to the increase in ambient temperature of the air passing over the devices. If the μA685 is operated without air flow, the change in electrical characteristics due to the increased die temperature must be taken into account.

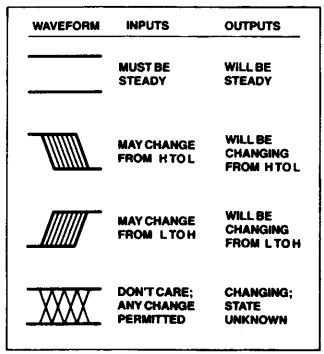
## Interconnection Techniques

All high speed ECL circuits require that special precautions be taken for optimum system performance. The μA685 is particularly critical because it features very high gain (60 dB) at very high frequencies (100 MHz). A ground plane must be provided for a good, low inductance, ground current return path. The impedance at the inputs should be as low as possible and lead lengths as short as practical. It is preferable to solder the device directly to the printed circuit board instead of using a socket. Open wiring on the outputs should be limited to less than one inch, since severe ringing occurs beyond this length. For longer lengths, the printed circuit interconnections become microstrip transmission lines when backed up by a ground plane, with a characteristic impedance of 50 to 150 Ω. Reflections will occur unless the line is terminated in its characteristic impedance. The termination resistors normally go to −2.0 V, but a Thevenin equivalent to V− can be used at some increase in power. Best results are usually obtained with the terminating resistor at the end of the driven line. The lower impedance lines are more suitable for driving capacitive loads. The supply voltages should be decoupled with RF capacitors connected to the ground plane as close to the device supply leads as possible.

## Timing Diagram




## Key To Timing Diagram

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**Note**

The set up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before $t_S$ will be detected and held; those occurring after $t_h$ will not be detected. Changes between $t_S$ and $t_h$ may or may not be detected.

## Definition Of Terms

**$V_{IO}$** **Input Offset Voltage** — That voltage which must be applied between the two input terminals through two equal resistances to obtain zero voltage between the two outputs.

**$\Delta V_{IO}/\Delta T$** **Average Temperature Coefficient Of Input Offset Voltage** — The ratio of the change in input offset voltage over the operating temperature range to the temperature range.

**$I_{IO}$** **Input Offset Current** — The difference between the currents into the two input terminals when there is zero voltage between the two outputs.

**$I_{IB}$** **Input Bias Current** — The average of the two input currents.

**$R_I$** **Input Resistance** — The resistance looking into either input terminal with the other grounded.

**$C_I$** **Input Capacitance** — The capacitance looking into either input terminal with the other grounded.

**$V_{CM}$** **Common Mode Voltage Range** — The range of voltages on the input terminals for which the offset and propagation delay specifications apply.

**CMR** **Common Mode Rejection** — The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

**PSRR** **Power Supply Rejection Ratio** — The ratio of the change in input offset voltage to the change in power supply voltages producing it.

**$V_{OH}$** **Output Voltage HIGH** — The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

$V_{OL}$ **Output Voltage LOW** — The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

$I+$ **Positive Supply Current** — The current required from the positive supply to operate the comparator.

$I-$ **Negative Supply Current** — The current required from the negative supply to operate the comparator.

$P_C$ **Power Consumption** — The power dissipated by the comparator with both outputs terminated in 50 Ω to −2.0 V.

## Switching Terms (see Timing Diagram)

$t_{PD+}$ **Input To Output HIGH Delay** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

$t_{PD-}$ **Input To Output LOW Delay** — The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{PD+(E)}$ **Latch Enable To Output HIGH Delay** — The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{PD-(E)}$ **Latch Enable To Output LOW Delay** — The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

$t_S$ **Minimum Set up Time** — The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

$t_h$ **Minimum Hold Time** — The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ **Minimum Latch Enable Pulse Width** — The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.

## Other Symbols

| | | | |
|---|---|---|---|
| $T_A$ | Ambient temperature | $V_T$ | Output load terminating voltage |
| $R_S$ | Input source resistance | $R_L$ | Output load resistance |
| $V_{CC}$ | Supply voltages | $V_{in}$ | Input pulse amplitude |
| $V+$ | Positive supply voltage | $V_{OD}$ | Input overdrive |
| $V-$ | Negative supply voltage | $f$ | Frequency |