FAIRCHILD
A Schlumberger Company

μA687 • μA687A
Dual Voltage Comparators

Linear Division Comparators

Description

The μA687 and μA687A are fast dual voltage comparators manufactured with an advanced high speed bipolar process that makes possible very short propagation delays (8.0 ns) with excellent matching characteristics. These comparators have differential analog inputs and complementary logic outputs compatible with most forms of ECL. The output current capabilities are adequate for driving terminated 50 Ω transmission lines. The low input offsets and short delays make these comparators especially suitable for high speed precision analog to digital processing.

Separate latch functions are provided to allow each comparator to be independently used in a sample and hold mode. The latch function inputs are designed to be driven from the complementary outputs of a standard ECL gate. If latch enable is HIGH and $\overline{\text{latch enable}}$ is LOW, the comparator functions normally. When latch enable is driven LOW and $\overline{\text{latch enable}}$ is driven HIGH, the comparator outputs are locked in their existing logical states. Should the latch function not be used, latch enable must be connected to ground.

The μA687 and μA687A are lead compatible with the AM687.

- **8.0 ns Maximum Propagation Delay At 5 mV Overdrive**
- **Complementary ECL Outputs**
- **50 Ω Line Driving Capability**

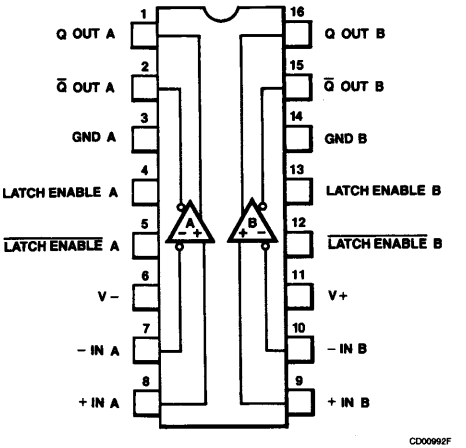
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	
Extended (μA687M/AM)	−55°C to +125°C
Industrial (μA687V/AV)	−30°C to +85°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Positive Supply Voltage	+7.0 V
Negative Supply Voltage	−7.0 V
Input Voltage	±4.0 V
Differential Input Voltage	±6.0 V
Output Current	30 mA
Minimum Operating Voltage	
(V+ to V−)	9.7 V

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram
16-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA687DM	6B	Ceramic DIP
μA687DV	6B	Ceramic DIP
μA687PV	9B	Molded DIP
μA687ADM	6B	Ceramic DIP
μA687ADV	6B	Ceramic DIP
μA687APV	9B	Molded DIP

μA687/AV, μA687AM

Electrical Characteristics Over the recommended operating temperature and supply voltage ranges, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition[1]	μA687/AV		μA687/AM		Units
			Min.	Max.	Min.	Max.	
V_{IO}	Input Offset Voltage	$R_S \leq 100\ \Omega$, $T_A = 25°C$	−3.0	+3.0	−2.0	+2.0	mV
		$R_S \leq 100\ \Omega$	−3.5	+3.5	−3.0	+3.0	
$\Delta V_{IO}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage[2]	$R_S \leq 100\ \Omega$	−10	+10	−10	+10	μV/°C
I_{IO}	Input Offset Current[2]	$25°C \leq T_A \leq T_{A\ Max}$	−1.0	+1.0	−1.0	+1.0	μA
		$T_A = T_{A\ Min}$	−1.3	+1.3	−1.6	+1.6	
I_{IB}	Input Bias Current	$25°C \leq T_A \leq T_{A\ Max}$		10		10	μA
		$T_A = T_{A\ Min}$		13		16	
V_{CM}	Common Mode Voltage Range		−3.3	+2.7	−3.3	+2.7	V
CMR	Common Mode Rejection	$R_S \leq 100\ \Omega$, $-3.3 \leq V_{CM} \leq +2.7$ V	80		80		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\ \Omega$, $\Delta V_S = \pm 5\%$	70		70		dB
V_{OH}	Output Voltage HIGH	$T_A = 25°C$	−0.960	−0.810	−0.960	−0.810	V
		$T_A = T_{A\ Min}$	−1.060	−0.890	−1.100	−0.920	
		$T_A = T_{A\ Max}$	−0.890	−0.700	−0.850	−0.620	
V_{OL}	Output Voltage LOW	$T_A = 25°C$	−1.850	−1.650	−1.850	−1.650	V
		$T_A = T_{A\ Min}$	−1.890	−1.675	−1.910	−1.690	
		$T_A = T_{A\ Max}$	−1.825	−1.625	−1.810	−1.575	
I+	Positive Supply Current			35		32	mA
I−	Negative Supply Current			48		44	mA
P_C	Power Consumption			485		450	mW

Switching Characteristics $V_{in} = 100$ mV, $V_{OD} = 5.0$ mV

Symbol	Characteristic	Condition[1]	μA687/AV		μA687/AM		Units
			Min.	Max.	Min.	Max.	
t_{PD}	Propagation Delay (μA687A)[2]	$T_{A\ Min} \leq T_A \leq 25°C$		8.0		8.0	ns
		$T_A = T_{A\ Max}$		10		12.5	
t_{PD}	Propagation Delay (μA687)[2]	$T_{A\ Min} \leq T_A \leq 25°C$		10		10	ns
		$T_A = T_{A\ Max}$		14		20	
t_S	Minimum Latch Set Up Time[2]	$T_A = 25°C$		4.0		4.0	ns

Notes

1. Unless otherwise specified V+ = +5.0 V, V− = −5.2 V, $V_T = -2.0$ V, and $R_L = 50\ \Omega$; all switching characteristics are for a 100 mV input step with 5.0 mV overdrive. The specifications given for V_{IO}, I_{IO}, I_{IB}, CMR, PSRR, t_{PD+} and t_{PD-} apply over the full V_{CM} range and for ±5% supply voltages. The μA687 and μA687A are designed to meet the specifications given in the table after thermal equilibrium has been established with a transverse air flow of 500 LFPM or greater.
2. Guaranteed, but not tested in production.