

μ A771 Operational Amplifier

Linear Division Operational Amplifiers

Description

This monolithic JFET Input Operational Amplifier incorporates well matched ion implanted JFETs on the same chip with standard bipolar transistors. The key features of this op amp are low input bias current in the sub nanoamp range plus high slew rate (13 V/ μ s typically) and wide bandwidth (3.0 MHz typically).

- Low Input Bias Current — 200 pA
- Low Input Offset Current — 100 pA
- High Slew Rate — 13 V/ μ s Typically
- Wide Bandwidth — 3.0 MHz Typically

Absolute Maximum Ratings

Storage Temperature Range

Ceramic DIP	-65°C to +175°C
Molded DIP and SO-8	-65°C to +150°C

Operating Temperature Range

Extended (μ A771AM, μ A771BM)	-55°C to +125°C
Commercial (μ A771C, μ A771AC, μ A771BC, μ A771LC)	0°C to +70°C

Lead Temperature

Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-8 (soldering, 10 s)	265°C

Internal Power Dissipation^{1, 2}

8L-Ceramic DIP	1.30 W
8L-Molded DIP	0.93 W
SO-8	0.81 W

Supply Voltage

Supply Voltage	± 18 V
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Differential Input Voltage

Differential Input Voltage	30 V
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Input Voltage³

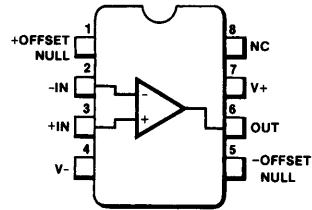
Input Voltage ³	± 16 V
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Output Short Circuit Duration

Output Short Circuit Duration	Indefinite
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Connection Diagram

8-Lead DIP and SO-8 Package (Top View)



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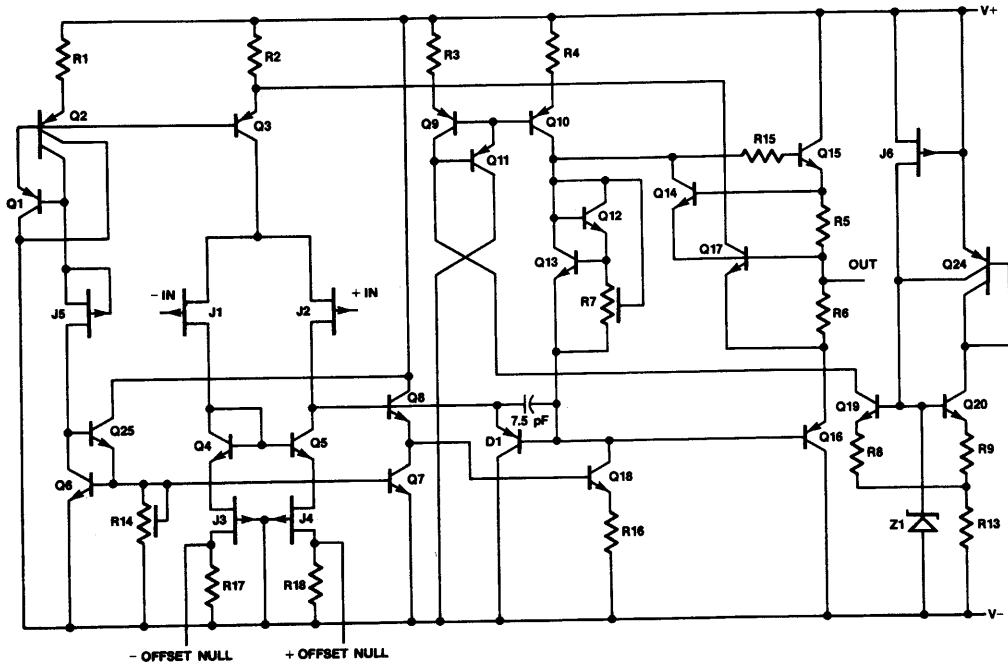
Order Information

Device Code	Package Code	Package Description
μ A771RC	6T	Ceramic DIP
μ A771SC	KC	Molded Surface Mount
μ A771TC	9T	Molded DIP
μ A771ARM	6T	Ceramic DIP
μ A771ARC	6T	Ceramic DIP
μ A771ASC	KC	Molded Surface Mount
μ A771ATC	9T	Molded DIP
μ A771BRM	6T	Ceramic DIP
μ A771BRC	6T	Ceramic DIP
μ A771BSC	KC	Molded Surface Mount
μ A771BTC	9T	Molded DIP
μ A771LRC	6T	Ceramic DIP
μ A771LSC	KC	Molded Surface Mount
μ A771LTC	9T	Molded DIP

Notes

1. $T_{J \text{ MAX}} = 150^\circ\text{C}$ for the Molded DIP and SO-8, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C . Above this temperature, derate the 8L-Ceramic DIP at $8.7 \text{ mW}/^\circ\text{C}$, the 8L-Molded DIP at $7.5 \text{ mW}/^\circ\text{C}$, and the SO-8 at $6.5 \text{ mW}/^\circ\text{C}$.
3. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Equivalent Circuit



EQ00051F

7

μA771

μA771 and μA771L

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA771			μA771L			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$V_{CM} = 0\text{ V}$, $R_S = 50\ \Omega$			10.0			15.0	mV
I_{IO}	Input Offset Current ¹	$V_{CM} = 0\text{ V}$, $T_J = 25^\circ\text{C}$			100			100	pA
I_{IB}	Input Bias Current ¹	$V_{CM} = 0\text{ V}$, $T_J = 25^\circ\text{C}$		50	200		50	200	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$	50	100		50	100		V/mV

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$

V_{IO}	Input Offset Voltage	$V_{CM} = 0\text{ V}$, $R_S = 50\ \Omega$			13			20	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input Offset Current ¹	$V_{CM} = 0\text{ V}$			4.0			4.0	nA
I_{IB}	Input Bias Current ¹	$V_{CM} = 0\text{ V}$			8.0			8.0	nA
I_{CC}	Supply Current				3.0			3.0	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11\text{ V}$, $R_S = 50\ \Omega$	70			70			dB
V_{IR}	Input Voltage Range		± 11	+15 -12		± 11	+15 -12		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10\text{ V}$ to $\pm 18\text{ V}$, $R_S = 50\ \Omega$	70			70			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10\text{ k}\Omega$	± 12			± 12			V
		$R_L = 2.0\text{ k}\Omega$	± 10			± 10			

μA771

μA771A and μA771B

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA771A			μA771B			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$V_{CM} = 0\text{ V}$, $R_S = 50\ \Omega$			2.0			5.0	mV
I_{IO}	Input Offset Current ¹	$V_{CM} = 0\text{ V}$, $T_J = 25^\circ\text{C}$			50			50	pA
I_{IB}	Input Bias Current ¹	$V_{CM} = 0\text{ V}$, $T_J = 25^\circ\text{C}$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current				2.8			2.8	mA
I_{OS}	Output Short Circuit Current			25			25		mA
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$	50	100		50	100		V/mV

The following specifications apply for $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$

V_{IO}	Input Offset Voltage	$V_{CM} = 0\text{ V}$, $R_S = 50\ \Omega$			4.0			7.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input Offset Current ¹	$V_{CM} = 0\text{ V}$			2.0			2.0	nA
I_{IB}	Input Bias Current ¹	$V_{CM} = 0\text{ V}$			4.0			4.0	nA
I_{CC}	Supply Current				3.0			3.0	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11\text{ V}$, $R_S = 50\ \Omega$	80			80			dB
V_{IR}	Input Voltage Range		± 11	+15 -12		± 11	+15 -12		V
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10\text{ V}$ to $\pm 18\text{ V}$, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10\text{ k}\Omega$	± 12			± 12			V
		$R_L = 2.0\text{ k}\Omega$	± 10			± 10			

μA771

μA771AM and μA771BM

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, unless otherwise specified.

DC Characteristics

Symbol	Characteristic	Condition	μA771AM			μA771BM			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage	$V_{CM} = 0\text{ V}$, $R_S = 50\ \Omega$			2.0			5.0	mV
I_{IO}	Input Offset Current	$V_{CM} = 0\text{ V}$, $T_J = 25^\circ\text{C}$			50			50	pA
I_{IB}	Input Bias Current	$V_{CM} = 0\text{ V}$, $T_J = 25^\circ\text{C}$		50	100		50	100	pA
Z_I	Input Impedance			10^{12}			10^{12}		Ω
I_{CC}	Supply Current				2.8			2.8	mA
V_{IR}	Input Voltage Range		± 11	+15 -12		± 11	+15 -12		V
CMR	Common Mode Rejection	$V_{CM} = \pm 11\text{ V}$, $R_S = 50\ \Omega$	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10\text{ V}$ to $\pm 18\text{ V}$, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$	50			50			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10\text{ k}\Omega$	± 12			± 12			V
		$R_L = 2.0\text{ k}\Omega$	± 10			± 10			

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$

V_{IO}	Input Offset Voltage	$V_{CM} = 0\text{ V}$, $R_S = 50\ \Omega$			5.0			8.0	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Sensitivity	$R_S = 50\ \Omega$		10			10		$\mu\text{V}^\circ/\text{C}$
I_{IO}	Input Offset Current ¹	$V_{CM} = 0\text{ V}$			20			20	nA
I_{IB}	Input Bias Current ¹	$V_{CM} = 0\text{ V}$			50			50	nA
I_{CC}	Supply Current				3.4			3.4	mA
CMR	Common Mode Rejection	$V_{CM} = \pm 11\text{ V}$, $R_S = 50\ \Omega$	80			80			dB
PSRR	Power Supply Rejection Ratio	$V_{CC} = \pm 10\text{ V}$ to $\pm 18\text{ V}$, $R_S = 50\ \Omega$	80			80			dB
A_{VS}	Large Signal Voltage Gain	$V_O = \pm 10\text{ V}$, $R_L \geq 2.0\text{ k}\Omega$	25			25			V/mV
V_{OP}	Output Voltage Swing	$R_L = 10\text{ k}\Omega$	± 12			± 12			V
		$R_L = 2.0\text{ k}\Omega$	± 10			± 10			

μA771 (Cont.)

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{ V}$, unless otherwise specified.

AC Characteristics

Symbol	Characteristic	Condition	All Grades			Unit
			Min	Typ	Max	
BW	Bandwidth	(Figure 2) $A_V = -10$		3.0		MHz
SR	Slew Rate	(Figure 1)		13		V/μs
e_n	Input Noise Voltage	$R_S = 100\ \Omega$, $f = 1000\text{ Hz}$		16		nV/√Hz
i_n	Input Noise Current	$f = 1000\text{ Hz}$		0.01		pA/√Hz

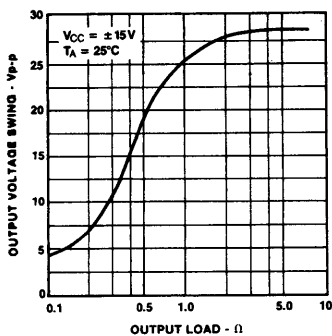
Note

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal

operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA}P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

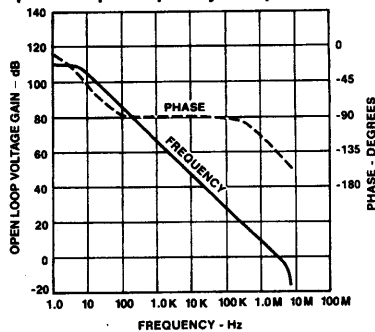
Typical Performance Curves

Output Voltage Swing vs Load Resistance



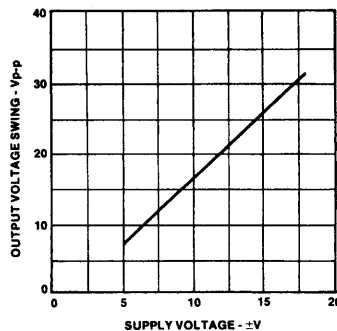
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Open Loop Frequency Response



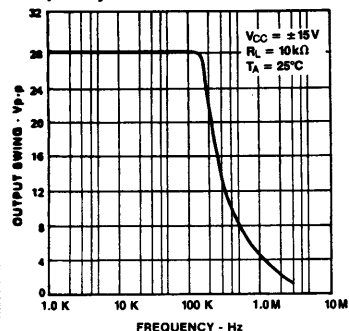
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Output Voltage Swing vs Supply Voltage



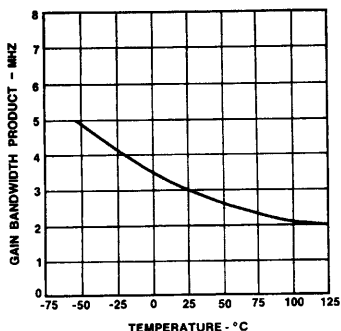
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Maximum Undistorted Output vs Frequency



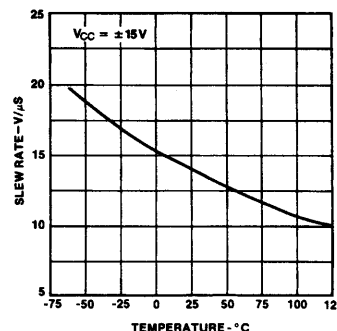
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Gain Bandwidth Product vs Temperature



PC02871F

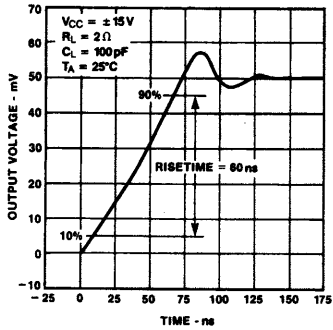
Slew Rate vs Temperature



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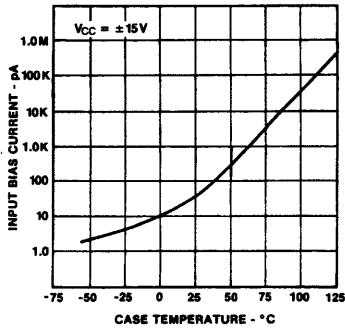
Typical Performance Curves (Cont.)

Small Signal Pulse Response



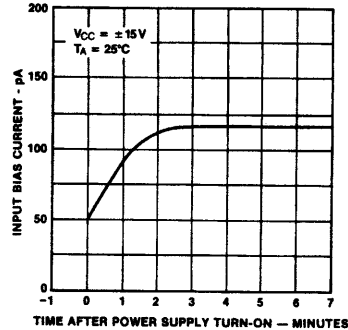
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Input Bias Current vs Case Temperature



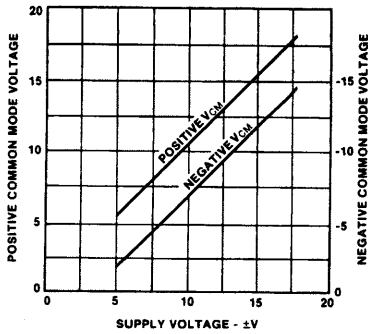
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Bias Current Warm up Change



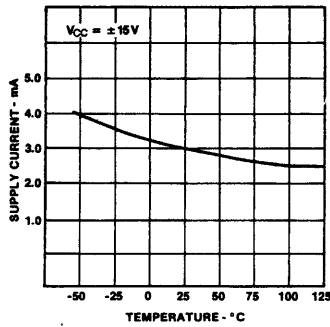
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Maximum Common Mode Input Voltage vs Supply Voltage



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Supply Current vs Temperature



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